Large-Signal FET Modeling based on Pulsed Measurements

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***Abstract* — The new FET model presented in this paper highlights a method through which complex current flow dynamics, arising from typical dispersion phenomena, can be modeled in equivalent circuits. Static and bias-dependant dynamic/pulsed currents are characterized using a new single mathematical expression and subsequently implemented into a large-signal circuit topology as a single current source. The model is based on a well-established conventional DC model and only minimal alteration is required. In this work we extend the range of validity to full large-signal operation including accurate prediction of nonlinear harmonic distortion and inter-modulation distortion (IMD) products. Furthermore, the single current source approach enhances the overall equivalent circuit topology's consistency with the physical device, a particularly favorable feature in such device models.**

***Index Terms* — FETs, intermodulation distortion, nonlinear circuits, MESFETs, power amplifiers, scattering parameters.**

I. Introduction

Accurate characterization of FET devices for modern communication system design requires highly accurate mathematical models of the device's main non-linearities. These include, most notably, the drain-source current Ids, the primary source of nonlinear distortion and IMD in amplifier circuits [1]. Large-signal performance of Ids models, in an equivalent circuit topology, must account for bias-dependant dispersion phenomena, including deep level traps and surface states, which often result in undesired transient effects in real FET devices [2]. Furthermore, various modulation schemes such as wide-band co-division multiple access (WCDMA), drive an amplifier to the extreme regions of the output I-V plane under large-signal excitation and consequently give rise to changing average or DC bias conditions of the amplifier [3]. Hence, device behavior can no longer be characterized by the bias point alone, as is the case in small-signal RF conditions.

Several efforts, similar to those in [4], have been proposed to account for DC/RF discrepancies. Typically these involve the inclusion of an extra current source in parallel with the DC Ids model. However, the mathematical expressions defining these elements are typically derived by performing integral operations on the algebraic discrepancies between DC and RF trans-conductance/output-conductance data deduced from S-parameters. Therefore they only represent the "local" properties of the device at the individual bias points [5].

I-V models derived from pulsed measurements overcome this problem as demonstrated by [6], where static and dynamic large-signal characterization of the device current flow was carried out under multi-bias pulsed I-V conditions. However, implementation still required a separate parallel current source in series with a relatively large capacitor, to account for low frequency dispersion, the physical existence of which, in an equivalent circuit topology, is quite questionable.

Recently, a new model called COBRA-PERU [7] was introduced and implemented using only one current source and a novel 4-terminal topology that models the back-gating and the transition between DC and RF, using dispersive networks in the gate and drain sides within the topology of the equivalent circuit. In related work [8], also based on pulsed measurements, we have demonstrated that by using a different form of the Ids equation, implemented into the same 4-terminal topology, one can predict not only DC and pulsed characteristics but also small-signal RF behavior.

In this paper a new equation for Ids is implemented into a 4-terminal topology. It demonstrates that by using only one current source based on pulsed measurements, it is now possible to predict the RF performance of the device under test (DUT) under large-signal multi-bias conditions, while accounting for a wide range of low-frequency dynamics. One-tone, two-tone and WCDMA simulations agree with the measured data and thus provide a validation of the essential methodology proposed in [7].

II. Model Formulation

The process of formulating a single expression for the pulsed current under multi-bias conditions was based around alterations to the existing COBRA model [4] as seen in (1-4).

$$Ids = f(Vgs_{DC}, Vds_{DC}, vgs_{PUL}, vds_{PUL}) \qquad (1)$$

$$= \beta(Vgs_{DC}, Vds_{DC}).V_{eff}^{p}.tanh(\alpha(Vgs_{DC}, Vds_{DC}) \times vds_{PUL}.(1+\zeta.V_{eff}))$$

where

$$p = \frac{\lambda(Vgs_{DC}, Vds_{DC})}{1+\mu.vds_{PUL}+\xi.V_{eff}} \qquad (2)$$

$$V_{eff} = \frac{1}{2}.\left(V_{gst} + \sqrt{V_{gst}^2 + \partial^2}\right) \qquad (3)$$

$$V_{gst} = vgs_{PUL} - (1+\beta_r^2).V_{TO}(Vgs_{DC}, Vds_{DC}) + \gamma.vds_{PUL} \qquad (4)$$

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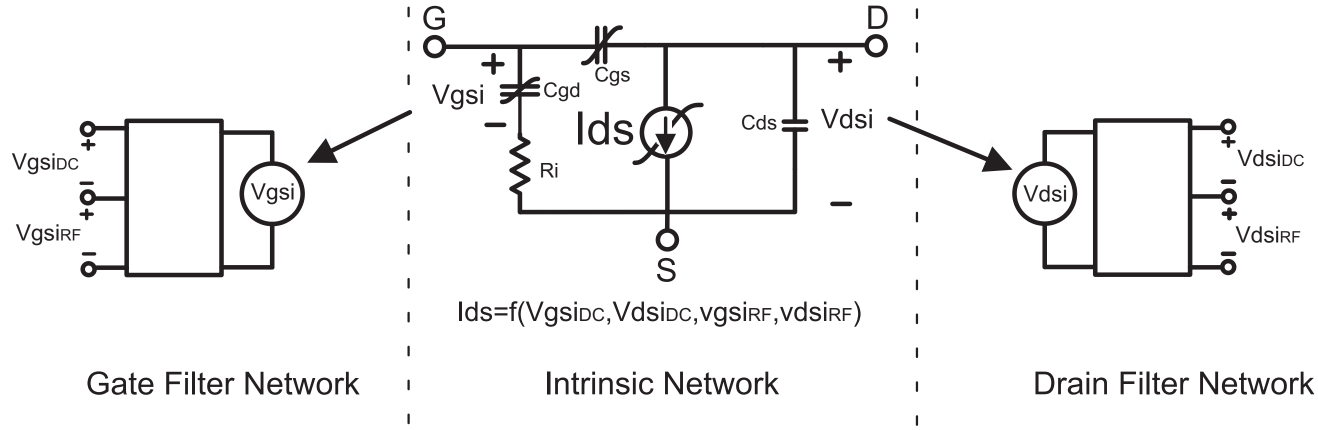

Fig. 1. Large-signal equivalent circuit intrinsic topology including drain and gate side filter networks.

The most notable aspect of this proposed model is its dependence on four voltages as opposed to just two, as is the case of the model in its original form. These voltages include the drain-source and gate-source DC bias voltages, Vds_{DC} and Vgs_{DC} respectively, and a further set of characterization variables, namely the drain-source and gate-source pulsed bias voltages, vds_{PUL} and vgs_{PUL} respectively. Further alterations include the introduction of DC bias dependencies to some of the COBRA model's original empirical parameters, including β, V_{to}, λ, and α. These alterations permit the modeling of pulsed currents from any DC bias point. The remaining parameters of the COBRA model, δ, ζ, γ, ξ, and μ were found not to vary significantly for the different sets of pulsed currents over the DC bias plane and were accordingly held constant.

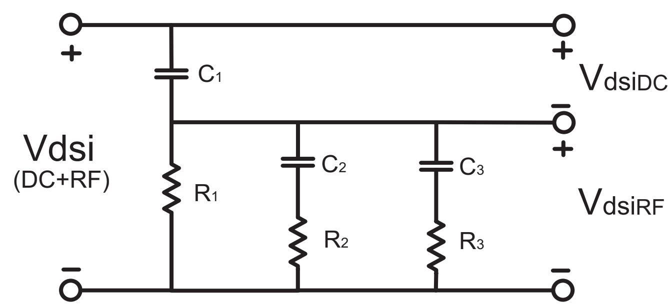

Fig. 2. Proposed drain filter network. A similar network was applied to the gate filter network. C1=100pF, C2=C3=150pF, R1=55MOhm, R2=5.6MOhm and R3=0.12MOhm.

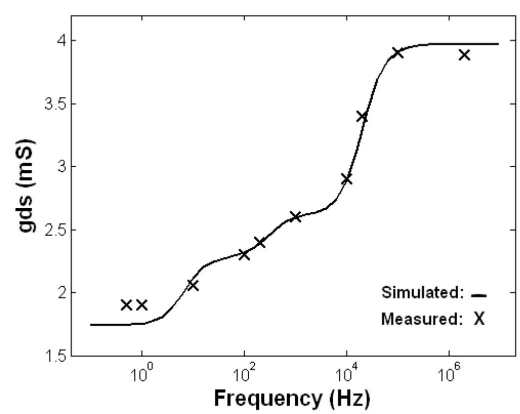

Fig. 3. Measured and simulated output-conductance dispersion at a DC bias point of Vgs=0.0V and Vds=3.0V.

III. Model Implementation

The circuit in Fig. 1 shows the complete large-signal intrinsic circuit implementation of the model within a CAD environment such as ADS. Having de-embedded the extrinsic parasitic elements, the trans-conductances and output-conductances, evaluated from the intrinsic S-parameters, were found to correspond to those determined from the pulsed I-V model [7]. In other words:

$$g_{ds}\Big|_{S-param} = g_{ds}\Big|_{pulsed} \ \ \& \ \ g_m\Big|_{S-param} = g_m\Big|_{pulsed} \quad (5)$$

Hence having established the validity of the pulsed nonlinear current source model (1) from small-signal analysis by (5), it could now be implemented into the large-signal topology as a single current source element now described by the following:

$$Ids = f(Vgsi_{DC}, Vdsi_{DC}, vgsi_{RF}, vdsi_{RF}) \quad (6)$$

Here, $Vgsi_{DC}$ and $Vdsi_{DC}$, and $vgsi_{RF}$ and $vdsi_{RF}$ represent the gate/drain-source DC and RF intrinsic voltages respectively. As one would expect, for correct simulation, access to these static and dynamic components was required. This was achieved using two multi-pole RC filter networks as shown in Fig. 1. The circuit topology for these networks can be seen in Fig. 2. It was synthesized such that it could effectively separate the static and dynamic components of the intrinsic voltage Vgsi and Vdsi and, more importantly, model the multi-time constant transitional behavior of dispersive parameters, including gm and gds, from DC to microwave frequencies as illustrated in Fig 3. Selection of the filter element values in Fig. 2 was obtained from analysis of the transient response generated by the DiVA pulsed I-V measurement system.

IV. Results And Analysis

In previous works, e.g. [4], as a DC model alone, the capabilities of the standard COBRA model were presented and its continuous nature and infinitely continuous derivatives have been demonstrated. Hence, an inheritance of this model's accurate performance capabilities in this work was expected, as the following results will clearly highlight. All measurements were performed on a GaAs MESFET transistor (NE76038).

Fig. 4 shows the measured and modeled pulsed I-V behavior from a DC bias of Vgs=-0.5V and Vds=2.5V. As one can see an excellent fit has been obtained throughout the pulsed IV plane, particularly around the knee, soft breakdown regions and, most importantly, around the bias point, thus preserving the static behavior of the DUT. Similar agreement was found from the majority of bias points throughout the bias plane.

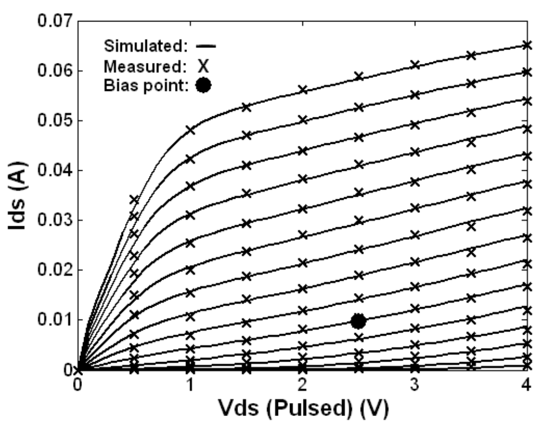

Fig. 4. Measured (X) and modeled (‒) pulsed I-V curves at a DC bias point of Vgs=-0.5V and Vds=2.5V. Vgs pulsed range from -1.0V to +0.4V in 0.1V steps. Vds pulsed range from 0.0V to 4.0 V in 0.5V steps.

To validate the small-signal RF performance of the model, Fig. 5 shows the simulated and measured S-parameters at a particular bias point. This kind of agreement, between measured and modeled S-parameters, is typical of what we have observed for DC bias points covering most of the bias plane.

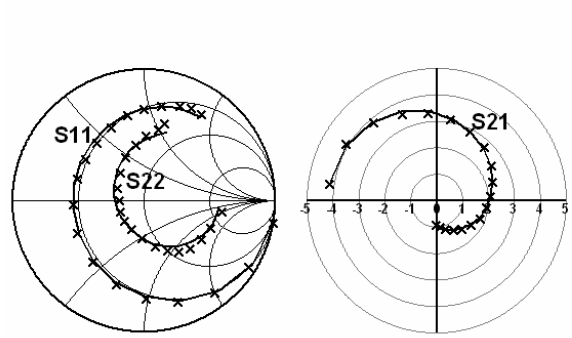

Fig. 5. Measured (X) and modeled (‒) S-parameters at a DC bias point of Vgs=-0.2V and Vds=2.5V and frequency range of 0.5GHz to 18.5GHz in 1.0GHz steps.

Large-signal characteristics of the model were verified by one and two-tone tests. All simulations were performed in ADS using the harmonic balance simulation tool. Fig. 6 represents both the measured and simulated one-tone excitation of the device at a bias of Vgs=-0.4V and Vds=2.0V. These results both emphasize the exceptional performance of the new model and validate the proposed (6) under small and large-signal conditions.

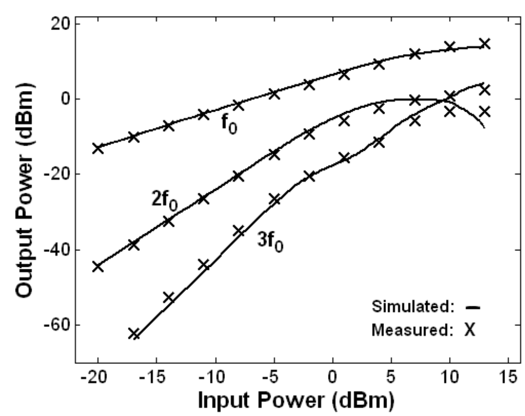

Fig. 6. Large-signal one-tone output power performance for a 2GHz signal at a DC bias point of Vgs=-0.6V and Vds=2.0V.

Furthermore, verification of the IMD performance of the model can be seen in Fig 7. For this test, two-tone measurements have been performed on the DUT with a tone spacing of 4MHz at a bias point of Vgs=-0.6V and Vds=3.0V. The model is seen to accurately predict the high order IMD products when driven by weakly and strongly nonlinear signals. A similar result can be observed in Fig 8, where the IMD performance is tested at a different bias point, further highlighting the validity of the model under multi-bias conditions. To date no significant IMD asymmetry has been observed for this device.

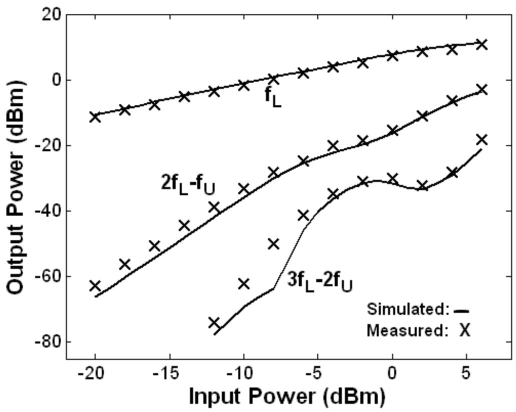

Fig. 7. Large-signal two-tone output power performance centered at 2GHz and tone spacing of 4MHz at a DC bias of Vgs=-0.6V and Vds=3.0V.

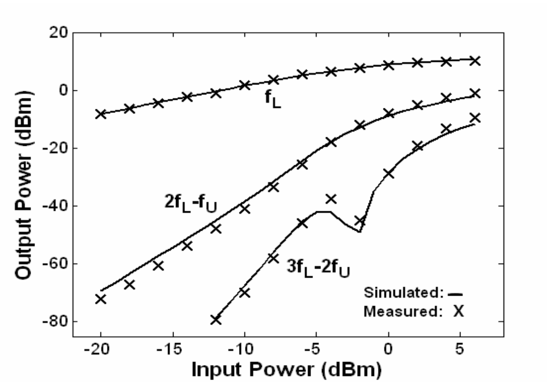

Fig. 8. Large-signal two-tone output power performance centred at 2GHz and tone spacing of 4MHz at a bias point of Vgs=-0.2V and Vds=2.0V.

The model has also been tested with real application based signals. A Third Generation Partnership Project (3-GPP) WCDMA signal excitation with a 3.84-Mchip/s chip rate at 2.14GHz was applied to the device at several input levels. The comparison between the measured and simulated behavior for an input excitation of -5dBm is depicted in Fig. 9. Outstanding correlation between the measured and modeled results of the output base-band time waveform can be observed.

IIV. Conclusion

A new large-signal model, based on pulsed measurements of microwave transistors, has been presented. A single expression, describing the complete dynamic and static characteristics of a FET device, has been formulated and then implemented as a single current source into a typical FET/HEMT equivalent circuit topology. Various aspects of the model prediction capabilities have been assessed including pulsed I-V, S-parameter and one and two-tone large-signal tests under multi-bias conditions. Finally the model was tested with a real application based WCDMA signal with analysis

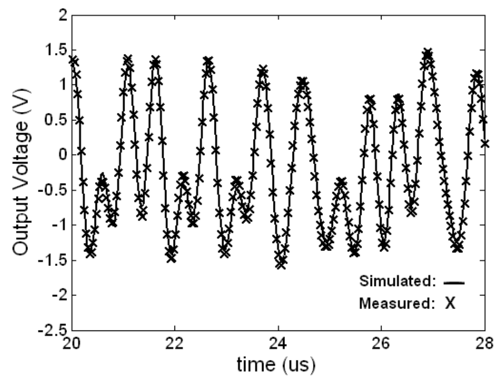

Fig. 9. Time domain base-band WCDMA signal excitation at a centre frequency of 2.14GHz and -0.5dBm input power level at DC bias of Vgs=-0.4V and Vds=2.5V.

focused on the base-band time domain signal. Excellent agreement between simulated and measured results has been presented. Currently, research work is now focused on some of the more complex aspects of the model's large-signal performance capabilities including memory effects as observed in other devices and device technologies.

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