Quantifying Distortion of RF Power Amplifiers for Estimation of Predistorter Performance

Paul J. Draxler^{1,2}, Anding Zhu³, Jonmei J. Yan², Pavel Kolinko², Donald F. Kimball², and Peter M. Asbeck²

¹ Qualcomm Inc., 5775 Morehouse Dr., San Diego, CA, USA
² University of California, San Diego, La Jolla, CA, USA
³ University College Dublin, Dublin 4, Ireland

Abstract — This paper demonstrates a method to quantify the accuracy of memory models and the effectiveness of digital predistortion of power amplifiers with memory. By using assumptions of periodic stationarity, coherent ensemble averaging and a stable measurement system, we are able to decompose the waveform distortion into memoryless, deterministic memory, and random memory contributions. We demonstrate how this can be used to evaluate the performance of a power amplifier and project its optimal performance with predistortion. We also show experimentally that the dynamic deviation reduction-based Volterra series digital predistortion technique has convergent behavior, moving towards these quantified targets when applied to a class AB power amplifier implemented with GaN FETs.

Index Terms — Behavioral modeling, linearization, power amplifier, predistorter, Volterra series.

I. INTRODUCTION

Many behavioral models and predistortion based linearization techniques for RF power amplifiers (PAs) have been introduced in recent years [1-3]. A significant problem for the practicing engineers is how to determine which model should be used for a given amplifier and how much improvement can be achieved with each type of digital predistorter (DPD). Specific questions include: will memoryless DPD be sufficient to achieve the specification or will memory effects need to be compensated? If so, what level of complexity does the memory compensation need to have to achieve the target specification?

In this paper, we present a measurement oriented distortion estimation technique to enable answering these questions. We also demonstrate a DPD algorithm with progressively better memory compensation which is applied experimentally to a power amplifier.

The rest of the paper is organized as follows. In section II, we present the details of the methodology that quantifies memoryless distortion, deterministic and nondeterministic memory in the PA. In section III, we briefly introduce the open loop DPD derived from *dynamic deviation reduction*-based Volterra series. In section IV, we test a class AB power amplifier that is driven with a WCDMA signal and present the results. This includes a series of DPD experiments which we

compare to the predictions, quantifying the performance levels.

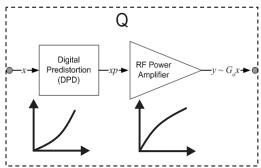


Fig. 1. A predistortion system

II. DISTORTION ESTIMATION

A technique has been previously presented in [4] that demonstrates the elimination of deterministic memory from a waveform by using multiple measurements, ensemble averages and successive approximations. In this section we present an extension of this technique which can be used to predict the optimal linearization targets for an amplifier throughout the DPD process. This is achieved by extracting a memoryless model, estimating the random components and using known waveforms to generate estimates of the total system performance (where the system includes both the predistortor and amplifier as shown in Fig. 1).

In the discrete complex envelope domain when a signal, x(n), is modified by the predistortion block to generate xp(n), which is applied to an amplifier, the output, y(n), is described as:

$$y(n) = G(n) \cdot xp(n)$$

$$G(n) = |G(n)| \cdot \exp(j\Theta(n))$$
(1)

where the function G(n) is the complex describing function of the amplifier's nonlinear gain, and $\Theta(n)$ specifies the phase response. In memoryless cases, |G(n)| and $\Theta(n)$ are functions of the current value of xp(n) only; however, the more general case results in a gain that is dependent on additional parameters or context. This context dependence is referred to as memory and has two components: deterministic and non-

deterministic. Following equation (1), we decompose the left hand side into three terms: a memoryless term, $y_{ml}(n)$, a deterministic memory term, $y_{mem}(n)$, and a non-deterministic term, $y_n(n)$ (which includes noise, non-reproducible memory, transient events, and other random events):

$$y(n) = y_{ml}(n) + y_{mem}(n) + y_n(n)$$
 (2)

The memoryless term can be determined with one measurement of a complex input sequence (such as a WCDMA signal) covering a wide range of input power levels, since this is the expected gain characteristic, or memoryless model, of the amplifier across the range of input envelope values. To form appropriate averages, we group values of input power into a set of bins centered around \hat{x}_i (for the ith bin), and then define:

$$y_{ml}(n) = \overline{G}(\hat{x}p) \cdot xp(n) \tag{3}$$

where:

$$\overline{G}(\hat{x}p) = E \left[\frac{y}{xp} \exp\left(j \cdot angle\left(\frac{y}{xp} \right) \right) | \hat{x}p | \right], \tag{4}$$

where $\hat{x}p$ are the input bins. The actual gain G(n), (1), and expected gain (4) define gain residue which can be used to quantify the memory effect and build the memory model.

In order to separate out the memory terms into the deterministic and non-deterministic components, we need to perform repeated measurements of the system operating on the same data. By looking at the output as a composite of a repeated memoryless component and deterministic memory component with a random component that is different from one waveform to the next, we can obtain an estimate of the non-deterministic memory term.

The deterministic memory term can be extracted by assuming that the sequence has periodic stationarity with the repeat length of the measurement sequence. This is only possible if the measurement is repeatable. This requires that the local oscillators of the upconverter and down converter have low phase noise, are phase and frequency locked to one another and the clocks on the DAC and ADC's are carefully controlled. The output of a periodically stationary system has an identical "context" each time a specific sample point is experienced. By taking the measurement repeatedly and performing proper time alignment on the output sequences we can obtain a sample by sample difference to quantify the level of waveform randomness. If for 2 repeated measurements with the same input data, xp(n), we obtain outputs $y_i(n)$, and $y_i(n)$, then an initial estimate of the non-deterministic component can be obtained:

$$y_{1n}(n) - y_{2n}(n) = y_1(n) - y_2(n) \tag{5}$$

where the non-deterministic term, $y_n(n)$, is a random variable (which, for a properly adjusted measurement system, we expect to be independent, identically distributed - iid). Ideally, it is a white noise signal with random phase, but can be

associated with other random discontinuous events or chaotic behavior. By performing a coherent averaging on a number of these outputs, one can generate a noise reduced estimate of the output waveform:

$$\frac{\sum_{i=1}^{N} y_i(n)}{N} = y_{ml}(n) + y_{mem}(n) + \frac{|y_n(n)|}{\sqrt{N}} \exp(j\vartheta(n))$$

where ϑ (n) is a uniform random variable between 0 and 2π . As we take more samples, we can a obtain more accurate estimate of the deterministic output signal and output random effects.

$$\frac{\sum_{i=1}^{N} y_i(n)}{N} = (y_{ml}(n) + y_{mem}(n))$$
 (6)

$$y_n(n) \approx y(n) - \frac{1}{N} \sum_{i=1}^{N} y_i(n)$$
 (7)

By quantifying and decomposing the output into these three terms, one can quantify the level of model completeness as well as perform estimates of different predistortion configurations. For example, if one would like the optimal memoryless performance for the output of the system, Q_{ml} , we can use equations (2) and (3) to get:

$$y_{Q_{ml}}(n) = G_o x(n) + y_{mem}(n) + y_n(n)$$
 (8)

where the constant amplification of the compensated system Q is G_o , the system gain term. For another example, with memory predistortion, the system, Q_{mem} , has compensated memory effects. If all memoryless distortion and deterministic memory have been removed, the output of the system becomes:

$$y_{Q_{more}}(n) = G_o x(n) + y_n(n)$$
. (9)

The remaining effect is the non-deterministic term which isn't compensated in the system.

Once we have these optimal performance targets for the amplifier, we can properly evaluate memory effect models and the associated predistortion algorithms relative to the performance specifications of the system.

III. DYNAMIC DEVIATION REDUCTION DPD

To validate the distortion evaluation methodology described in section II, we employ an open loop DPD technique [5] as our test. This DPD approach was derived from the *dynamic deviation reduction*-based Volterra series [4], that allows compensation for nonlinear distortion and memory effects induced by RF power amplifiers in a very efficient and effective way. In this approach, the Volterra model is pruned

by controlling the order of dynamics involved in the system, which dramatically simplifies the system implementation. For example, if only the first-order dynamics are taken into account, the DPD function in the discrete complex envelope domain can be written as

$$\tilde{u}(n) = \sum_{k=0}^{\frac{P-1}{2}} \sum_{i=0}^{M} \tilde{g}_{2k+1,1}(i) |\tilde{x}(n)|^{2k} \tilde{x}(n-i)$$

$$+ \sum_{k=1}^{\frac{P-1}{2}} \sum_{i=1}^{M} \tilde{g}_{2k+1,2}(i) |\tilde{x}(n)|^{2(k-1)} \tilde{x}^{2}(n) \tilde{x}^{*}(n-i)$$

$$(10)$$

where $\tilde{x}(n)$ and $\tilde{u}(n)$ are the complex envelopes of the input and the output, respectively, and $\tilde{g}_{2k+1,j}(\cdot)$ is the complex Volterra kernel of the system. (·)* represents the complex conjugate operation and $|\cdot|$ returns the magnitude. Based on the *p*th-order post-inverse theory [6], the parameters of this DPD can be directly estimated from the measured input and output of the PA with a simple off-line characterization process.

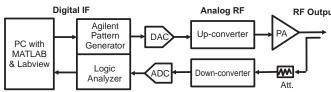


Fig. 2. The experimental test bench

IV. EXPERIMENTAL RESULTS

A Nitronex GaN HEMT based PA operated in Class AB was used for experimental measurements. The device was biased with Vds=28V, Vgs=-1.49V, and an idle drain current of 0.8A, at 1.95 GHz. The system includes a pattern generator, DAC, an upconverter, and the output was captured with a logic analyzer after going through a down-converter and an ADC as shown in Fig.2. Seven predistortion configurations are evaluated, where the system (predistorter + amplifier) was excited with a WCDMA waveform (decrested to a peak to average ratio (PAR) of 7.5 dB). A summary of these results is presented in Table I. The sampling rate is 15.36 MHz and there are 9360 samples.

For each test case, the input waveform was modified by the specified predistorter (P is the polynomial order and M is the memory depth), then applied to the PA. Then, four output measurements were aquired. From the PA input and output waveforms, an estimate of the memoryless waveform was made (8) and the normalized root mean squared error (NRMSE [7]) to the target waveform was computed and reported (Est. ML in Table I). From each pair of output measurements, the NRMSE of the deterministic memory limit (N=2 est. Non-Det in Table I) is computed (5).

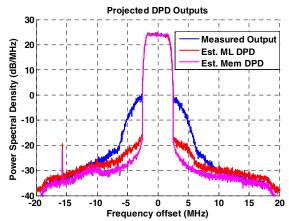


Fig. 3. Measured, estimated memoryless DPD and estimated deterministic memory compensation limits.

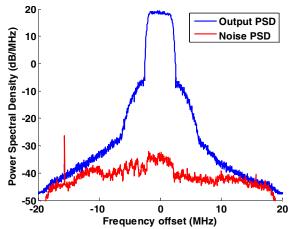


Fig. 4. Original PSD of the measurement and the estimated nondeterministic waveform PSD.

The optimal system performance estimates (8,9) are calculated and the power spectral densities calculated for these are presented in Fig. 3. Fig. 4 shows the PSD of the output waveform and the non-deterministic waveform obtained from equation (5). The low value of the non-deterministic waveform (of order 0.9%) demonstrates the high accuracy of the test signal generator and output captured. Comparable values are measured with "through" connections from input to output. The power in the error signal can be quantified by the NRMSE.

One thing to note is that one of the local oscillators is responsible for the spurious tone in Fig. 3-4 at a -16MHz offset (i.e. LO leakage). We believe this is a 3rd order intermodulation product from the LO.

Experiment 1, on Table I, predicts a target of a NRMSE of 6.03% for the memoryless DPD floor, even though the current measurement has a NRMSE of 15.2% when no predistortion is applied. Experiment 2 and 3 have increasing predistorter polynomial order, and yield similar memoryless DPD performance estimates. Experiment 3 with P= 11 performs within 0.05% of the memoryless DPD goal. Measurements 3-7 have the same polynomial order (P=11), but a progression in

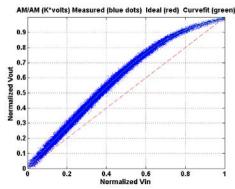


Fig. 5a. Amplifier sample performance without DPD.

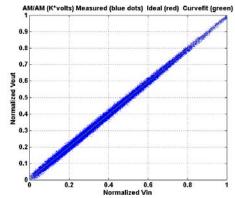


Fig. 5b. Amplifier performance with 11th order memoryless DDR DPD (Experiment #3).

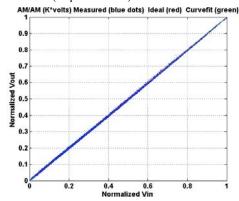


Fig. 5c. DPD + Amplifier performance when DPD has 11th order, 4 memory taps DDR DPD (Experiment #7).

the memory tap depth (M=0,1,2,3,4). The benefit of additional terms is diminishing by experiment 7, although the estimates reveal that a portion of the memory effect remains to be compensated. The overall DPD AMAM performance progression through these experiments is presented in Fig.5.

TABLE I. – Experimental Results and Performance Estimates

Exp	P	М	Pin (dBm)	Po (dBm)	NRMSE (%)		
					Meas	Est.	N=2 est.
						ML	Non-Det
(1)	0	0	27.77	40.98	15.2	6.03	0.7-08
(2)	5	0	25.28	38.86	6.45	6.08	0.6-0.9
(3)	11	0	25.2	38.78	6.13	6.08	0.6-1.0
(4)	11	1	25.17	38.75	4.42	6.20	0.5-1.0
(5)	11	2	25.13	38.74	1.91	6.36	0.6-1.0
(6)	11	3	25.25	38.8	1.80	6.36	0.7-1.0
(7)	11	4	25.26	38.76	1.78	6.36	0.6-1.0

V. CONCLUSION

An experimental methodology has been demonstrated to quantify the performance floor of memoryless and memory modeling and predistortion. With this approach, one can quantify the nonlinear distortion and memory effects in power amplifiers and evaluate the extent to which these effects can be compensated by specific linearization algorithms. With one measurement of the system with a complex modulated waveform, one can estimate the expected gain characteristics of the amplifier and the limits of memoryless DPD. With additional measurements, one can determine the repeatability of the measurement system and estimate the deterministic memory effects that could be compensated.

ACKNOWLEDGEMENT

The authors wish to acknowledge the assistance and support of the Center for Wireless Communications, Qualcomm Inc., Science Foundation Ireland, Agilent Technologies, and Nitronex.

REFERENCES

- [1] M. Isaksson, D. Wisell, D. Ronnow, "A comparative analysis of behavioral models for RF power amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 1, pp. 348-359, Jan. 2006.
- [2] J.C. Pedro, S.A. Maas, "IEEE Trans. Microw. Theory Tech., vol. 53, no. 4, pp. 1150-1163, April 2005.
- [3] J. Wood and D.E. Root, Eds., Fundamentals of Nonlinear Behavioral Modeling for RF and Microwave Design. Norwood, MA: Artech House, 2005.
- [4] A. Zhu, J. C. Pedro, and T. J. Brazil, "Dynamic deviation reduction-based Volterra behavioral modeling of RF power amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 12, pp. 4323-4332, Dec. 2006.
- [5] A. Zhu, P. Draxler, J. Yan, T.J. Brazil, D.F. Kimball, and P.M. Asbeck, "Open loop digital predistorter for RF power amplifiers using dynamic deviation reduction-based Volterra series" submitted to IEEE Trans. Microw. Theory Tech.
- [6] M. Schetzen, *The Volterra and Wiener Theories of Nonlinear Systems*, reprint ed. Malabar, FL: Krieger, 2006.
- [7] P. Draxler, J. Deng, D. Kimball, I. Langmore, P.M. Asbeck, "Memory Effect Evaluation and Predistortion of Power Amplifiers," 2005 IEEE MTT-S Digest., TH2B, 2005