A Unified Approach to Charge-Conservative Capacitance Modelling in HEMTs

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***Abstract*—The voltage dependence of high electron mobility transistor (HEMT) gate-source- and gate-drain capacitance is described by a set of equations based on a unified charge-conservative model approach. The model is applied to a low-noise GaAs pseudomorphic-HEMT (pHEMT) technology as well as its power variant. In terms of topology and parameters, the new expressions resemble the Curtice drain current model. They provide a globally accurate description of nonlinearities in HEMT capacitance.**

***Index Terms*—Modulation-doped field effect transistors (MODFETs), semiconductor device modelling.**

I. Introduction

In MONOLITHIC microwave integrated circuit (MMIC) design, high model quality is one of the most obvious requirements for reducing development costs and time to market, particularly when carried out in comparatively expensive technologies. Compared to the Si metal-oxide-semiconductor field-effect transistor (MOSFET), today's III-V high electron mobility transistor (HEMT) technologies feature more pronounced nonlinearities in their electrical behaviour. Due to the complex epitaxial layer structures and associated physical properties, device level models dedicated to efficient circuit design are most appropriately carried out on an analytical, semi-empirical basis. In this context, the voltage dependence of gate capacitance constitutes the major reactive nonlinearity, often comparable in importance to the contribution of drain current for the accurate description of device dynamics.

II. Unified Model Formulation

In any FET device, the charge density in the channel is opposed by charge of equal magnitude and opposite polarity on the gate terminal, forming the total gate charge, which itself is a function of the terminal voltages V_{gs} and $V_{ds} = V_{gs} - V_{gd}$. Physically, the channel charge is distributed across the transistor gate length. In the equivalent circuit based modelling approach, the total gate charge is divided between (and attributed to) the gate-source- and gate-drain terminals. The entities extractable from S-parameter characterization are the capacitances between these terminals, together with their bias voltage dependencies: $C_{gs}(V_{gs}, V_{gd})$ and $C_{gd}(V_{gs}, V_{gd})$. For the capacitance to stem from a single channel charge, the capacitance model expressions need to satisfy the charge-conservation criterion [1], [2]

$$\frac{\partial C_{gs}(V_{gs}, V_{gd})}{\partial V_{gd}} - \frac{\partial C_{gd}(V_{gs}, V_{gd})}{\partial V_{gs}} = 0. \tag{1}$$

If this condition is not met, not only are the underlying device physics violated, but the simulator may run into convergence problems. While physical models like Statz–Pucel [3] and [4] have been proposed for FET charge and capacitance, they suffer from the same restrictions in terms of accuracy and global validity as do the drain current models. Especially in the case of advanced heterostructure devices such as the HEMTs investigated here, empirical models are resorted to for the development of models dedicated to circuit design.

Typically, such nonlinear capacitance equations are made up of terms which depend solely on the respective terminal voltage and others that contain both voltages (2). In the case of HEMT type devices, the former part, term D in (2), accounts for fringing capacitance, Schottky diode junction capacitance as well as the channel charge build-up arising from a change in the gate voltage at zero V_{ds} (3). Separate parameters may be provided for C_{gs} and C_{gd} to account for unsymmetry in the device geometry, e.g. due to intentional gate placement close to the source region. The remaining, interdependent terms F_2 and G_2 describe the V_{ds}-dependence of the gate capacitance. In terms of modelling, this is the crucial and most demanding part, since charge-conservation needs to be observed

$$\begin{aligned} C_{gs}(V_{gs}, V_{gd}) &= D(V_{gs}) + F_2(V_{gs}, V_{gd}) \\ C_{gd}(V_{gs}, V_{gd}) &= D(V_{gd}) + G_2(V_{gs}, V_{gd}) \end{aligned} \tag{2}$$

$$\begin{aligned} D(V) = C_{\mathrm{p}} &+ \frac{C_1}{\left(1 - \frac{V}{V_{\mathrm{bi}}}\right)^m} \\ &+ C_2\left(1 + \tanh\left(\kappa(V - V_{\mathrm{t2}})\right)\right). \end{aligned} \tag{3}$$

A generalized form can be written as (4) and (5), representing a unified approach to the charge-conservative modeling of FET capacitance and allowing for a variety of expressions $C_S(V_{gs})$ and $F_3(V_{ds})$ to describe the dependence on V_{gs} and V_{ds}, respectively. Charge-conservation is observed for any C_S and F_3, since (6) holds. The particular form of the interdependent terms adopted in this work [see (7) and (8)] is similar to the basic empirical drain current equation of Curtice [5]

$$\begin{aligned} F_2(V_{gs}, V_{gd}) = C_S(V_{gs}) \cdot F_3(V_{gs} - V_{gd}) - \frac{\partial C_S(V_{gs})}{\partial V_{gs}} \\ \cdot \int F_3(V_{gs} - V_{gd}) \partial V_{gd} \end{aligned} \tag{4}$$

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$$G_2(V_{gs},V_{gd}) = -C_S(V_{gs})\cdot F_3(V_{gs}-V_{gd}) \tag{5}$$

$$\begin{aligned}\frac{\partial C_{gs}}{\partial V_{gd}} &= C_S(V_{gs})\cdot(-1)\cdot\frac{\partial F_3(V_{gs}-V_{gd})}{\partial(-V_{gd})}\\ &\quad-\frac{\partial C_S(V_{gs})}{\partial V_{gs}}\cdot F_3(V_{gs}-V_{gd})\\ &= -C_S(V_{gs})\cdot\frac{\partial F_3(V_{gs}-V_{gd})}{\partial V_{gs}}\\ &\quad-\frac{\partial C_S(V_{gs})}{\partial V_{gs}}\cdot F_3(V_{gs}-V_{gd}) = \frac{\partial C_{gd}}{\partial V_{gs}}\end{aligned} \tag{6}$$

$$\begin{aligned}F_2(V_{gs},V_{gd}) &= C_S(V_{gs})\cdot(1+\tanh(\iota[V_{gs}-V_{gd}-V_{t4}]))\\ &\quad-\frac{\partial C_S(V_{gs})}{\partial V_{gs}}\\ &\quad\cdot\left(V_{gd}-\frac{1}{\iota}\ln(\cosh[\iota(V_{gs}-V_{gd}-V_{t4})])\right)\end{aligned} \tag{7}$$

$$\begin{aligned}G_2(V_{gs},V_{gd}) &= -C_S(V_{gs})\\ &\quad\cdot(1+\tanh(\iota[V_{gs}-V_{gd}-V_{t4}]))\end{aligned} \tag{8}$$

$$\begin{aligned}\frac{\partial C_{gs}}{\partial V_{gd}} &= \frac{\partial C_{gd}}{\partial V_{gs}}\\ &= -C_S(V_{gs})\cdot\iota\cdot\operatorname{sech}^2(\iota[V_{gs}-V_{gd}-V_{t4}])\\ &\quad-\frac{\partial C_S(V_{gs})}{\partial V_{gs}}\\ &\quad\cdot(1+\tanh[\iota(V_{gs}-V_{gd}-V_{t4})])\,.\end{aligned} \tag{9}$$

The term C_S corresponds to the saturation current I_S. The expression employed for C_S follows closely the definition of saturation current in drain current models

$$C_S(V_{gs}) = C_3\cdot V_{\text{eff}}^{\psi} \tag{10}$$

$$V_{\text{eff}} = \frac{1}{2}\left(V_{gs}-V_t+\sqrt{(V_{gs}-V_t)^2+\theta^2}\right) \tag{11}$$

where C_3 is a capacitance constant and V_{eff} corresponds to the "gate overtravel," derived from the threshold voltage V_t. The transition from the linear- to the saturated operating region, i.e., term F_3 in (4) and (5) for both C_{gs} and C_{gd} is described by a tanh() function. The charge-conservation criterion applied to the above equations yields (9). This set of equations represents a generalized form of similar capacitance expressions, such as [6] and [7] for an RF CMOS transistor technology. The full capacitance model based on the foregoing equations is applied to several HEMT technologies in the following.

III. Model Application

The capacitance model is incorporated in a full nonlinear FET model topology. Measured capacitance is obtained from multibias S-parameter extraction, carried out in a 100-nm low-noise GaAs pHEMT process (UMS PH15) with a cutoff frequency f_t of 110 GHz as well as its power variant (PPH15) with an f_t of 75 GHz. Fig. 1 shows extracted and modelled capacitance of a $2\times 20\ \mu$m GaAs power device, both for constant V_{ds} and constant V_{gs}, covering the IV plane from sub-threshold to active- and linear to saturated regimes.

Of particular interest is the observation of a local minimum of C_{gs}, when plotted versus V_{gs}. These characteristics are observed in all HEMT technologies. A possible physical interpretation [8] divides total capacitance of a modulation-doped field effect transistors (MODFET) gate structure into individual contributions from the 2 DEG and the Schottky junction. With increasing V_{gs} the 2 DEG capacitance drops, since the carrier concentration in the 2 DEG reaches an equilibrium and is no longer modulated by the gate potential due to the onset of carrier accumulation in the parasitic MESFET channel of the supply layer.

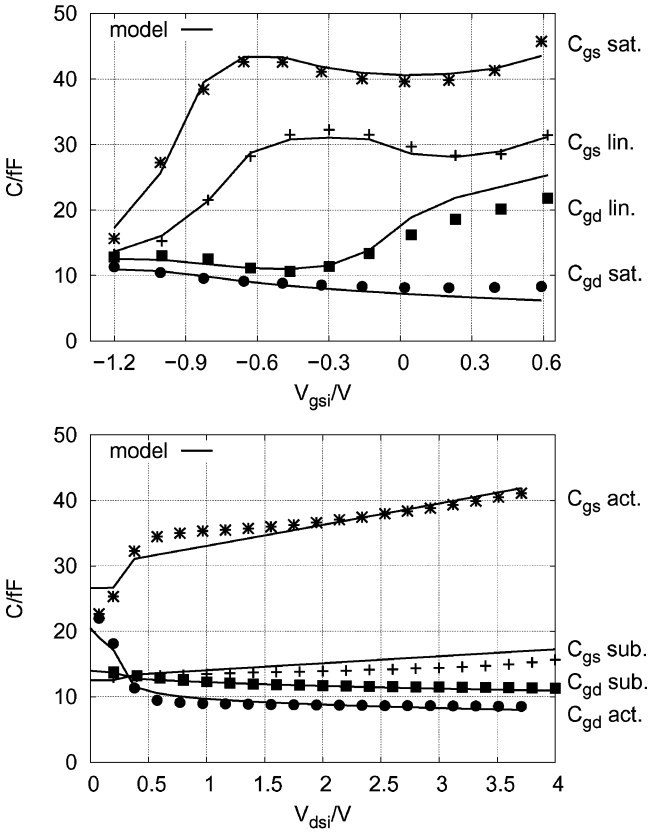

Fig. 1. Capacitance in a $2\times 20\,\mu$m GaAs power device. Versus V_{gs} in the linear and saturated region (top). Versus V_{ds} in subthreshold and active $(g_{\mathrm{m,max}})$ region (bottom).

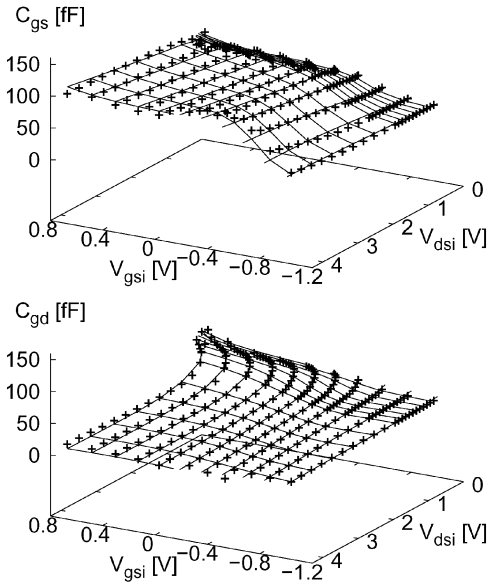

Fig. 2. Measured and modelled C_{gs} (top) and C_{gd} (bottom) in a $2\times 50\ \mu$m low-noise GaAs pHEMT versus terminal voltages.

Demonstrating the universal suitability of the model, Fig. 2 shows its application to a 2×50 μm low-noise GaAs pHEMT device. The model provides a globally accurate description of the measured capacitance nonlinearities over the full IV plane. The global root-mean-square deviation of the model, normalized to the measured values, is 6.1%.

REFERENCES

[1] D. E. Root, S. Fan, and J. Meyer, "Technology independent large signal non quasi-static FET models by direct construction from automatically characterized device data," in *Proc. 21st Eur. Microw. Conf.*, Stuttgart, Germany, Sep. 1991, pp. 927–932.

[2] A. D. Snider, "Charge conservation and the transcapacitance element: an exposition," *IEEE Trans. Education*, vol. 38, no. 4, pp. 376–379, Nov. 1995.

[3] H. Statz, P. Newman, I. Smith, R. Pucel, and H. Haus, "GaAs FET device and circuit simulation in SPICE," *IEEE Trans. Electron Devices*, vol. 34, no. 2, pp. 160–169, Feb. 1987.

[4] S. D'Agostino and A. Betti-Berutto, "Physics-based expressions for the nonlinear capacitances of the MESFET equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 42, no. 3, pp. 403–406, Mar. 1994.

[5] W. R. Curtice and M. Ettenberg, "A nonlinear GaAsFET model for use in the design of output circuits for power amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-33, no. 12, pp. 1383–1394, Dec. 1985.

[6] B. OhAnnaidh and T. J. Brazil, "A globally-continuous, charge-conservative, non-linear equivalent circuit model for RF MOSFETs," in *Proc. 11th GaAs Symp. Eur. Microw. Week*, Munich, Germany, Sep. 2003, pp. 65–68.

[7] M. Wren and T. J. Brazil, "Enhanced prediction of pHEMT nonlinear distortion using a novel charge conservative model," in *IEEE MTT-S Int. Dig.*., Jun. 2004, pp. 31–34.

[8] P. Roblin and H. Rohdin, *High-Speed Heterostructure Devices*. Cambridge, U.K.: Cambridge Univ. Press, 2002.