# DC and Large-Signal Microwave MOSFET Model Applicable to Partially-Depleted, Body-Contacted SOI Technology

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***Abstract* — A new compact DC and large-signal physics-based non-quasi-static (NQS) MOSFET model is proposed, suitable for partially-depleted body-tied silicon-on-insulator (SOI) MOSFETs. The developed four-terminal nonlinear model is comprised solely of fully-continuous explicit expressions that allow for quick simulation times and accurate intermodulation distortion analysis. Nonlinear depletion capacitances, as well as short-channel effects such as drain-induced barrier lowering, have been included, while the self-heating effects of SOI MOSFETs are modeled using a first-order thermal RC circuit. NQS distributed channel behaviour is accounted for by using a segmented channel model allowing the model in principle to operate up to high mm-wave frequencies. The model is verified for DC and large signal one-/multi-tone operation as well as through WCDMA measurements.**

***Index Terms* — Compact model, large-signal, nonlinear, silicon-on-insulator (SOI) MOSFETs.**

## I. Introduction

Silicon-on-insulator (SOI) technology is becoming increasingly important for RF/microwave applications due to its superior performance over bulk CMOS technology. The main comparative advantages of SOI MOSFETs relate to higher speeds, increased integration densities, and a higher current drive [1], [2]. While much research has been presented on DC and small-signal SOI modeling, relatively little has been done for large-signal models. Large-signal RF models are just as important as small-signal models, as they are used, for example, in the design of mixers and power amplifiers. High frequency operation requires the development of non-quasi-static (NQS) models to account for the temporal relaxation of the inversion and depletion charges [3]. Chan *et al.* [4] account for such NQS effects by adding Elmore resistances in series with the gate-source and gate-drain capacitances to model the distributed RC delay of the channel. While this method is relatively simple to implement, it only retains the lowest frequency pole of the original RC network. A recently proposed model [5] uses the spline-collocation technique to account for the NQS effects. Although accurate, it is rather complex to implement.

In this paper, we present a new four-terminal compact MOSFET model that is experimentally verified to be suitable for partially-depleted (PD) body-tied (BT) SOI MOSFETs. The model is based on a simple voltage-dependent saturating charge density expression [6] that is fully continuous between all operating regimes. NQS effects are accounted for by using a segmented channel model [7], [8], which automatically gives full consistency between large- and small-signal simulations. Numerous improvements have been added to the basic model in [6], including nonlinear depletion capacitances and short-channel effects such as drain-induced barrier lowering (DIBL). The proposed model also includes a thermal RC circuit to account for the self-heating effects (SHE) associated with SOI MOSFETs [3]. Further, a nonsingular electron velocity-field relation is used to ensure that the current is continuous around the $V_{DS}$ = 0 V region, an important requirement for analog circuit design. For the first time, the subthreshold DC characteristic and intermodulation distortion (IMD) capabilities of the charge model are demonstrated.

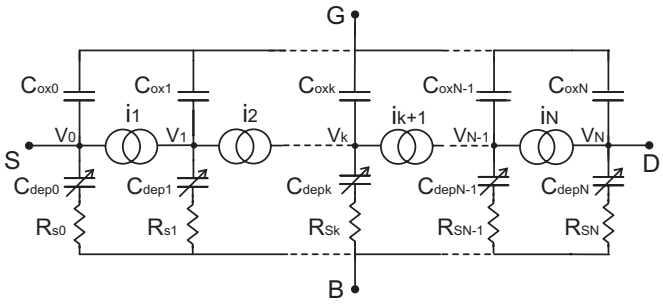


Fig. 1. Intrinsic channel model with N channel segments.

## II. Model Formulation

The intrinsic channel model proposed for this paper is shown in Fig. 1. The current sources in Fig. 1 are given by

$$i_k = -\mu(k,t)Wq(k,t)\frac{v(k,t)-v(k-1,t)}{h} \qquad (1)$$

where $k$ is the channel position, $k$ = 0, 1, …. $N$, $N$ being the number of channel segments, $\mu(k,t)$ is the position dependent channel mobility, $W$ is the channel width, $v(k,t)$ is the bulk-referenced channel voltage at position $k$, $h=L/N$ is the length of each channel segment, where $L$ is the channel length, and $q(k,t)$ is the channel charge density per unit area for segment $k$. The mobility expression in (1) is given by [7], [9]

$$\mu(k,t) = \frac{\mu_0}{\left(1+\theta v_{Geff}(t)\right)\left(1+\delta_0(k,t)\dfrac{|E(k,t)|}{E_C(t)}\right)} \qquad (2)$$

where $\mu_0$ is the low-field mobility, $\theta$ is a constant that accounts for mobility reduction due to high vertical fields, $v_{Geff}(t)$ is an effective ($v_{GB}(t)$-$V_T$) voltage [10], $V_T$ being the threshold voltage, $E(k,t)$ is the lateral electric field, $E_C(t) = v_{sat}(1+\theta v_{Geff}(t))/\mu_0$ is the critical electric field at which velocity saturation occurs, where $v_{sat}$ is the saturation velocity, and $\delta_0(k,t)$ is a semi-empirical correction factor given by [9]

$$\delta_0(k,t) = \frac{|v(k,t)-v(k-1,t)|}{|v(k,t)-v(k-1,t)|+g_h E_C(t)L} \tag{3}$$

where $g_h$ is an empirically adjustable parameter. The $\delta_0(k,t)$ term in (2) ensures that the mobility model is fully continuous around $V_{DS}$ = 0 V, an important requirement, for example, in IMD analysis for mixer design. The expression for $q(k,t)$ in (1) derives its origin from detailed analysis of the charge in the region near the drain in saturation using the two-dimensional physical simulator provided by Silvaco Corp. The concentration of electrons at the surface was shown to decrease toward the drain, and these electrons were pushed away from the surface and into the bulk. This consequently caused the current to flow in a "subsurface" path [7, section 6.2]. It was therefore necessary to incorporate the total charge, and not just the surface charge, to model this two-dimensional current. The developed charge density expression is [6]

$$q(k,t) = -C_{ox}\left(v_{Geff}(t) - \frac{\left([v(k,t)+v(k-1,t)]/2\right)v_{Geff}(t)}{\alpha\left([v(k,t)+v(k-1,t)]/2\right)+v_{Geff}(t)}\right) \tag{4}$$

where $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the oxide capacitance per unit area, $\varepsilon_{ox}$ is the permittivity of the oxide, $t_{ox}$ is the oxide thickness, and $\alpha$ is an empirical constant used to control the degree of saturation of the charge density expression. $v_{Geff}(t)$ in (4) provides a continuous smooth expression for $q(k,t)$ from weak inversion into strong inversion. It is important to note that (4) is also fully continuous between the linear and saturation regimes.

Threshold voltage is given by [3]

$$V_T = V_{T0} - \frac{\sigma_o}{1+\exp\{(V_{GB}-V_{\sigma t})/V_\sigma\}}V_{DS} \tag{5}$$

where $V_{T0}$ is the extracted threshold voltage at low $V_{DS}$ and the second term accounts for DIBL. Another important short-channel effect is channel length modulation (CLM) [3], [7], which is accounted for by multiplying (1) by $(1+\lambda_{CLM}v_a(k,t))$, where $\lambda_{CLM}$ is the CLM factor and $v_a(k,t)$ is the average value of the node voltages on either side of the channel segment.

SOI MOSFETs suffer significantly from SHE because of the thick buried oxide underneath the silicon layer [3], although advantageous electrically, dis-improves the thermal properties. The temperature dependence of the mobility is given by [10]

$$\mu_{eff}(k,t,T_{ch}) = \mu(k,t)\left(T_{ch}(t)/T_{amb}\right)^m \tag{6}$$

where $T_{amb}$ is the ambient temperature, $T_{ch}(t)$ is the channel temperature, and $m$ is the temperature coefficient of the mobility. The temperature rise of the channel can be modeled using an equivalent RC circuit. The average dissipated power in the channel has been used to estimate the increase in channel temperature, which is given by [3]

$$\left(T_{ch}(t)-T_{amb}\right) = i_N\left[v(N,t)-v(0,t)\right]R_{TH} \tag{7}$$

where $R_{TH}$ is the thermal resistance of the RC network. $T_{ch}(t)$ is calculated from (7) and substituted back into (6) to calculate the new channel mobility. The temperature in the channel also affects other parameters, such as the electron velocity. However for simplicity we choose to model all temperature effects with (7) and an appropriate value for $R_{TH}$. The value of $R_{TH}$ is verified by comparing the simulated conductance at DC and high frequencies, where the thermal effects are negligible, with the measured values.

The oxide capacitances in Fig. 1 are given by $C_{ox}Wh$. The nonlinear depletion capacitances are given by [7]

$$C_{depk}(t) = \frac{\sqrt{2q\varepsilon_s N_A}}{\kappa+2\sqrt{|\phi_s(t)+v(k,t)|}}Wh \tag{8}$$

where $\varphi_s(t)$ is the surface potential, $\kappa$ is included to aid convergence in the simulator, $\kappa << 1$, $q$ is the magnitude of the electron charge, $\varepsilon_s$ is the permittivity of the semiconductor, and $N_A$ is the substrate doping. To avoid the iterative implicit calculation of $\varphi_s(t)$ in (5) we have adopted a simplified approximation to relate $\varphi_s(t)$ to the gate voltage: When the gate voltage is equal to the flat-band voltage there is zero band bending and $\varphi_s(t)$ = 0 V [7]. With increasing gate voltage $\varphi_s(t)$ is assumed to increase nearly linearly until the channel becomes strongly inverted, at which point $\varphi_s(t)$ is taken to saturate to a near constant value, which is greater than the traditionally assumed value of twice the Fermi potential [7]. This simple $\varphi_s(t)$-$v_{GB}(t)$ curve can easily be approximated by an equation of the form

$$\phi_S(t) = A\,Tanh\left(Bv_{GB}(t)+C\right)+D \tag{9}$$

where $A$, $B$, $C$, and $D$ are optimized constants to fit (9) to the $\varphi_s(t)$-$v_{GB}(t)$ curve. Substituting (9) into (8) replaces the implicit equation with an explicit equation that is fast to solve. Finally, the substrate loss is modeled using the $R_{Sk}$ resistances, whose values are extracted from small-signal measurements.

## III. Model Verification

The Gummel Symmetry test [11] can be used to assess the symmetry of a model. Fig. 2 shows the results of the Gummel Symmetry test on the proposed model and the BSIM3SOI model. As can be seen, the second derivative of the proposed model is fully continuous and equal to zero at Vx = 0 V. This is a direct result of referencing all voltages to the bulk node. The BSIM3SOI model, on the other hand, is discontinuous at Vx = 0 V and fails the test for symmetry. This failure is attributed to a source-referenced threshold voltage and to a singularity in the velocity-field relation [11].

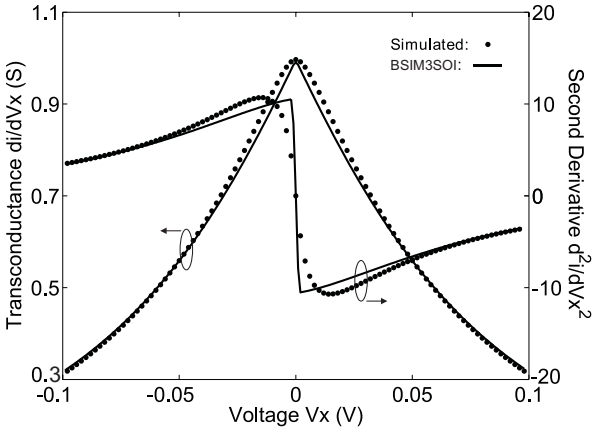


Fig. 2. Transconductance for proposed model (dots) and BSIM3SOI model (solid line) versus Vx. Also shown is the second derivative. The discontinuity in the BSIM3SOI model is obvious.

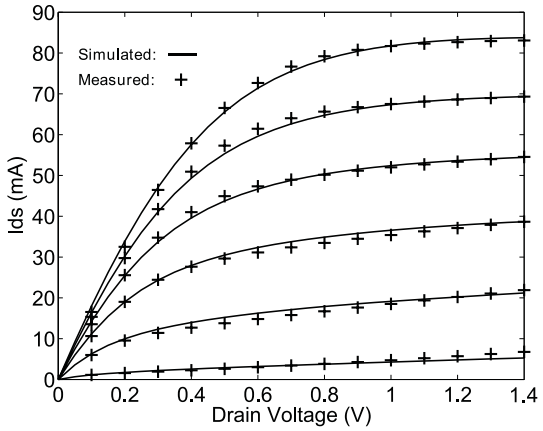


Fig. 3. Measured (crosses) and simulated (solid lines) DC characteristic. Gate voltages range from 0.4 V up to 1.4 V in steps of 0.2 V.

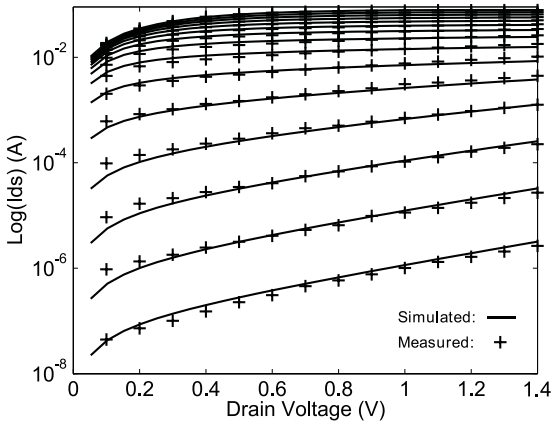


Fig. 4. Measured (crosses) and simulated (solid lines) log($I_{DS}$)-$V_{DS}$ characteristic. Gate voltages range from 0 V up to 1.4 V in steps of 0.1 V.

Measurements were performed on an N-type SOI PD BT MOSFET. The transistor had a channel length of 0.13 μm, with 30 gate fingers connected in parallel, each of width 4 μm, a front and back gate oxide thickness of, respectively, 2 nm and 400 nm, and a silicon thickness of 150 nm. The body was connected to the source. A MOSFET of this type allows us to use the original charge model developed for a bulk MOSFET in [6] to model the SOI device, since the body is tied to the source, and the silicon thickness is sufficiently deep for the charge to behave in a similar manner to the bulk device. The front gate oxide thickness, $t_{ox}$, is replaced with an effective electrical oxide thickness to incorporate the quantum mechanical effects associated with thin oxides. Based on a substrate doping density of $10^{17}$ $cm^{-3}$ and a polysilicon doping density of $9x10^{19}$ $cm^{-3}$, the electrical oxide thickness was extracted to be 2.9 nm [12]. Simulations, with $N$ = 5, were performed using Agilent's Advanced Design Simulator, where Symbolically Defined Devices were used to model the nonlinear current sources and depletion capacitances.

Fig. 3 shows the comparison of the simulated DC $I_{DS}$-$V_{DS}$ characteristic with the measured results, while Fig. 4 shows the subthreshold current characteristic. As shown in the figures, very good agreement is observed in the plots for the entire region of gate and drain bias. Note that all extrinsic parasitics are included in the model and have been extracted from small-signal S-parameter measurements.

Each additional channel segment adds just 20% of the simulation time of the single channel segment, which is much lower than other segmented models e.g. [8]. The model is computationally efficient because all of the equations are explicitly dependent on the voltages, avoiding any computationally-intensive iterative loops.

The dominant source of nonlinearity in the device is the channel current. To test the nonlinear capabilities of the model a 2 GHz tone from a 50 generator was applied to the gate of the device and the output power dissipated by the 50 load was measured at the fundamental, 2nd, and 3rd harmonics. Fig. 5 shows the comparison between the measured and simulated results. As shown, the model predicts the linear and nonlinear output powers with very good accuracy.

A two-tone test was then performed on the device to assess the model's ability to predict IMD. Two signals, centered around 2 GHz and with a tone spacing of 2 MHz, were applied at the input of the device. Fig. 6 shows the measured and modeled output powers at the lower fundamental, 3rd, and 5th order intermodulation (IM) powers. As can be seen, the model predicts the IM powers with reasonable accuracy.

An even more complicated distortion pattern at the output is obtained by applying a WCDMA signal at the input. An Agilent E4438C was used to generate a 3GPP-compliant WCDMA signal excitation with a 3.84-Mchip/s chip rate at 2.14 GHz. The WCDMA signal was applied with an input power of –15 dBm. A sample of the measured and simulated time-domain output voltages are shown in Fig. 7. As can be seen, even in this demanding case, the model shows excellent agreement with measurements.

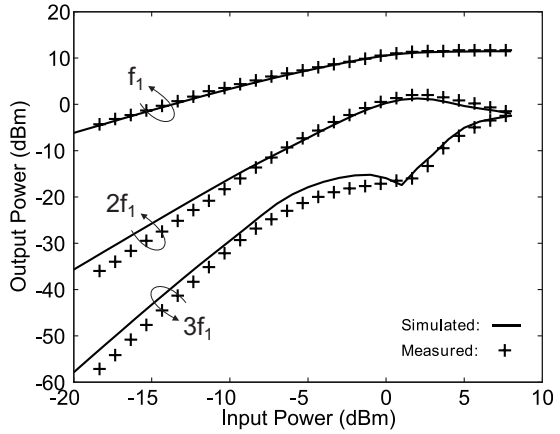


Fig. 5. Measured (crosses) and simulated (solid lines) output powers versus swept input power for a one-tone test for $V_{GS} = V_{DS} = 1.0$ V.

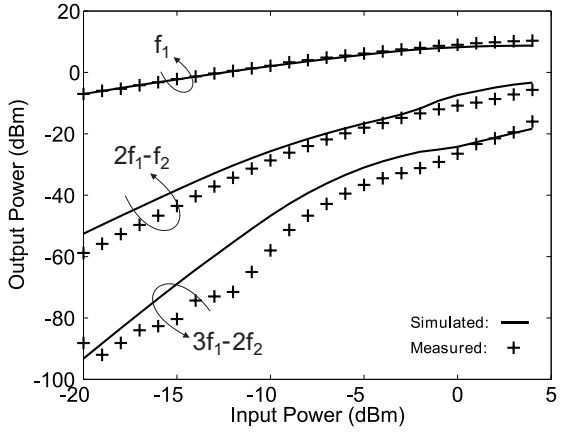


Fig. 6. Measured (crosses) and simulated (solid lines) 1st, 3rd, and 5th order lower IMD products of a two-tone test for $V_{GS} = V_{DS} = 1.2$ V.

## IV. Conclusion

A new DC and large-signal model has been presented and experimentally verified for use on PD BT SOI MOSFETs. The novelty of the model stems from the combination of different modeling techniques and the inclusion of important physical effects to create a fully continuous nonlinear model. For the first time, the subthreshold DC capabilities of the charge model have been demonstrated and proven to give excellent agreement with the measured results. The nonlinear and IMD predictabilities of the model have also been investigated and shown to accurately reproduce the measured characteristics.

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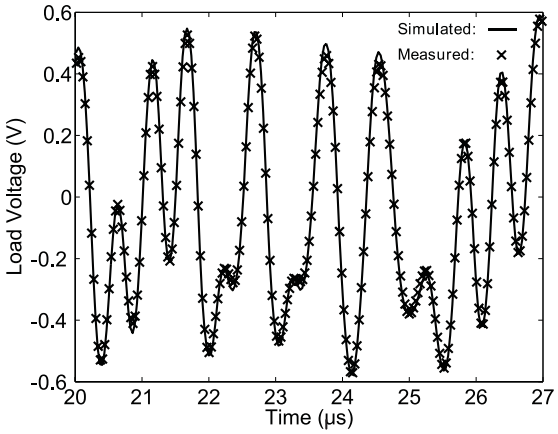


Fig. 7. Measured (x) and simulated (solid line) output waveforms for a WCDMA input signal for $V_{GS} = V_{DS} = 1.0$ V.

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