Experimental Class-F Power Amplifier Design Using Computationally Efficient and Accurate Large-Signal pHEMT Model

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***Abstract*—This paper presents an experimental high-efficiency class-F power amplifier (PA) design, which integrates Rhodes's efficient low-pass matching network topology with the charge conservative, robust, and accurate WREN/COBRA nonlinear pseudomorphic high electron-mobility transistor (pHEMT) model for optimal drain efficiency. Large-signal model verification is undertaken where one-tone, load–pull, and wireless code-division multiple-access baseband time-domain tests are compared for simulated and experimental cases. Following a detailed theoretical analysis, a class-F matching network is proposed that suppresses the necessary load harmonics and delivers maximum drain efficiency. Utilizing the GaAs pHEMT model in computer-aided design, a microstrip matching network layout was generated and built at 2 GHz. The drain efficiency recorded for the first-pass effort was 70.5% with the use of no post-fabrication circuit tuning. Excellent agreement is also observed between the PAs simulated and measured performance, thus highlighting the advantages of an accurate device model in PA design.**

***Index Terms*—Amplifier, class F, nonlinear modeling, pseudomorphic high electron-mobility transistor (pHEMT).**

I. Introduction

RF POWER amplifier (PA) efficiency is of critical importance in modern mobile communication systems. An increase in PA efficiency allows for a considerable reduction in mobile handset size and prolongs battery lifetime and reliability.

Various techniques in enhancing PA efficiency have been developed over the years and are mentioned in the literature [1]–[3]. It is now well established that high efficiency can be obtained with the appropriate dc operating conditions and matching load network. A robust and effective method is the class-F form of amplification, where an exact load harmonic strategy leads to a marked improvement in performance.

For a successful first-pass and efficient design, which employs computer-aided design (CAD) techniques, a reliable nonlinear device model is essential. A class-F PA places extreme operating conditions on the transistor with the device overdriven and biased at pinchoff. Consequently, there is an increased emphasis on the large-signal model, which is required to design the output matching networks.

In this paper, we describe in detail the design and fabrication of an experimental hybrid class-F PA at 2 GHz. The transistor used in the design is a Filtronic LP6836P70 packaged GaAs pseudomorphic high electron-mobility transistor (pHEMT) device. In Section II, we briefly introduce the large-signal pHEMT model. The model is based on an equivalent-circuit approach and employs robust globally continuous equations to describe the nonlinear circuit elements. The capacitances are based on a novel single-charge formulation that ensure charge conservation. A full verification of the large-signal model is highlighted in Section III following implementation in Agilent's ADS circuit simulator. In Section IV, a recently published [4] theoretical concept on class-F matching network design is introduced and then validated using simulation results. This method offers a simple more realizable output configuration compared to other existing methods [5] and can account for the effects of higher harmonic frequencies. Finally, in Section V, we extend the analysis of Section IV and describe the design and implementation of the microstrip prototype class-F PA. A wide range of test results are presented, comparing experimental data to simulation results.

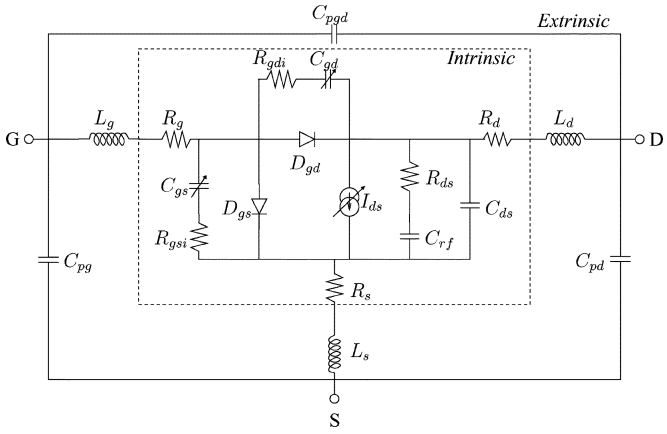

Fig. 1. Equivalent-circuit model for microwave pHEMTs.

II. Large-Signal Model

The first step in devising a nonlinear equivalent-circuit model is to embrace a particular form of model topology. The equivalent circuit of the Filtronic 0.25-μm AlGaAs/InGaAs/AlGaAs packaged pHEMT transistor is presented in Fig. 1 including both the extrinsic parasitic elements (C_{pg}, C_{pd}, C_{pgd}, L_g, L_d, and L_s) and the bias-dependent intrinsic model elements. The gate structure of the pHEMT forms a Schottky barrier to the semiconductor contact and this is represented by the presence

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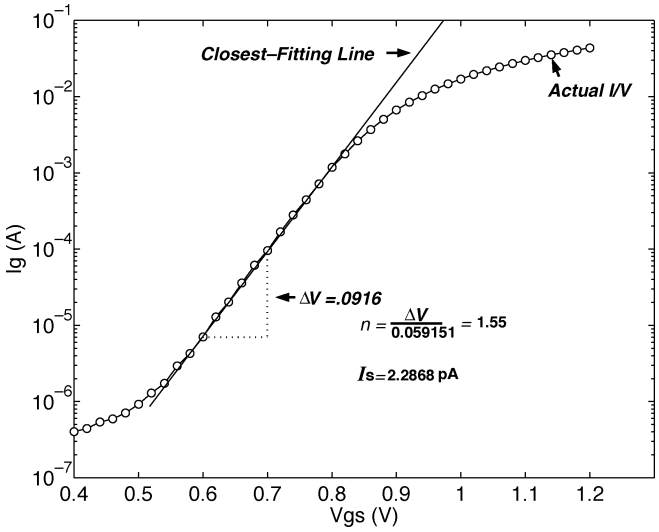

Fig. 2. Extraction of Schottky diode parameters using forward-bias gate current measurements. The ideality factor N and the gate junction current parameter were calculated to be 1.55 and 2.28 pA, respectively.

of the gate–source $(D_{\rm gs})$ and gate–drain $(D_{\rm gd})$ Schottky diodes in our model. The resistors $R_{{\rm gd}i}$ and $R_{{\rm gs}i}$ are modeled as linear elements and help describe non-quasi-static effects seen at high frequencies.

The main nonlinearities associated with the model are the nonlinear capacitances $C_{\rm gs}(V_{\rm gs}, V_{\rm ds})$ and $C_{\rm gd}(V_{\rm gd}, V_{\rm ds})$ and the nonlinear drain current source $I_{\rm ds}(V_{\rm gs}, V_{\rm ds})$. These functions can be described by analytical expressions, which have a dual voltage dependency and are dependent on the intrinsic terminal voltages of the device. Frequency-dispersion effects have been found to be very small for this device technology and are, therefore, sufficiently represented by the inclusion of the $(R_{\rm ds}, C_{\rm rf})$ series in parallel with the nonlinear drain current generator $I_{\rm ds}$ [6].

A. Gate Schottky Diode Model

The two diodes in the gate circuit are suitably described by the conventional thermionic emission-diffusion Schottky current model (1) with parameters I_S and N representing the gate junction current parameter and Schottky junction ideality factor, respectively, [7] as follows:

$$I_{{\rm gs},d} = I_S \left[\exp\left(\frac{V_{{\rm gs},d}}{N.V_t} \right) - 1 \right]. \tag{1}$$

Precise extraction of these parameter values have been shown to be important for overall large-signal model exactness. They play a key role in characterizing the knee area of the dc characteristics, especially when the gate is forward biased under large-signal excitation [8], as is the case when the device is used in high-efficiency PA design. Parameter values for the device-under-test (DUT) were easily determined, as shown in Fig. 2, by fitting the diode equation to forward gate–source bias measurements of the gate current taken at a drain–source voltage of zero.

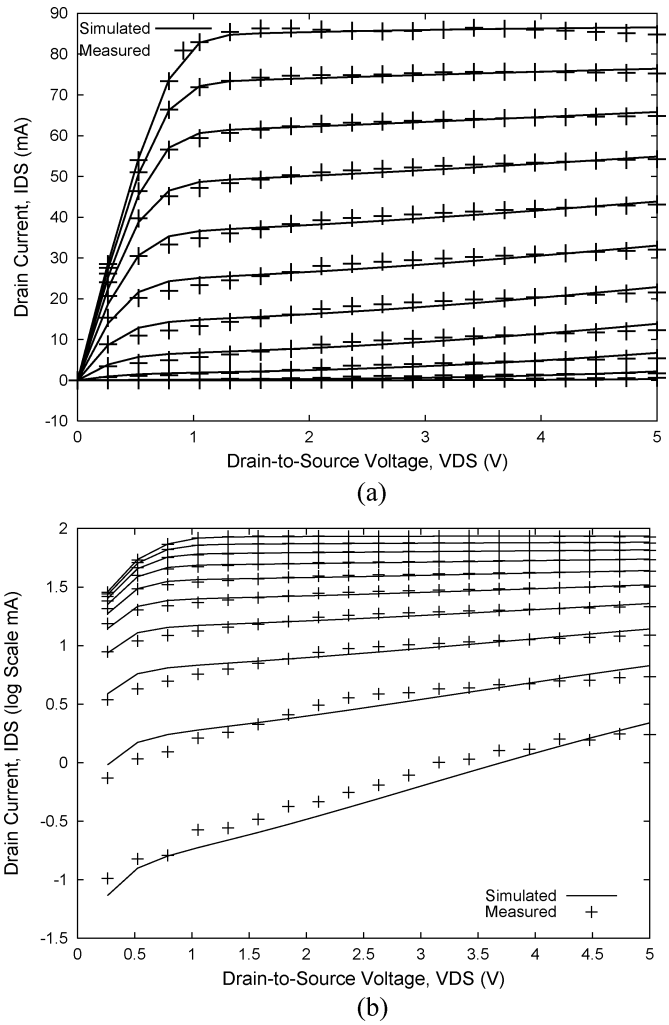

Fig. 3. Comparison between the measured and simulated dc characteristics showing: (a) an excellent global fit over entire dc bias range and (b) highlighting the COBRA model fidelity at pinchoff levels.

B. DC Model

The COBRA model [9] developed for MESFET and pHEMT devices is employed here to represent the nonlinear drain current source. The model presents a closed-form analytical expression (2) as follows:

$$\begin{aligned} &I_{\rm ds}(V_{\rm gs}, V_{\rm ds}) \\ &\quad = \beta V_{\rm eff}^{\lambda} \sqrt{1+\mu \cdot V_{\rm ds}^2 + \xi \cdot V_{\rm eff}} \tanh\left[\alpha V_{\rm ds}(1+\zeta V_{\rm eff})\right] \\ &V_{\rm eff} \\ &\quad = \frac{\left(V_{\rm gs} - V_{TO} + \gamma . V_{\rm ds} + \sqrt{(V_{\rm gs} - V_{to} + \gamma . V_{\rm ds})^2 + \delta^2}\right)}{2} \end{aligned} \tag{2}$$

where V_{TO} is the pinchoff voltage and β, μ, λ, ξ, α, ζ, γ, and δ are model parameters with no physical meaning, but allow for efficient extraction from dc measurements in a Levenberg–Marquardt numerical optimization algorithm. The ability of the model to accurately represent the device behavior in the knee, linear, and saturation regions of the drain characteristic is highlighted in Fig. 3(a), while the semilogarithm graph of Fig. 3(b) emphasizes the excellent convergency properties of the COBRA model in the pinchoff region.

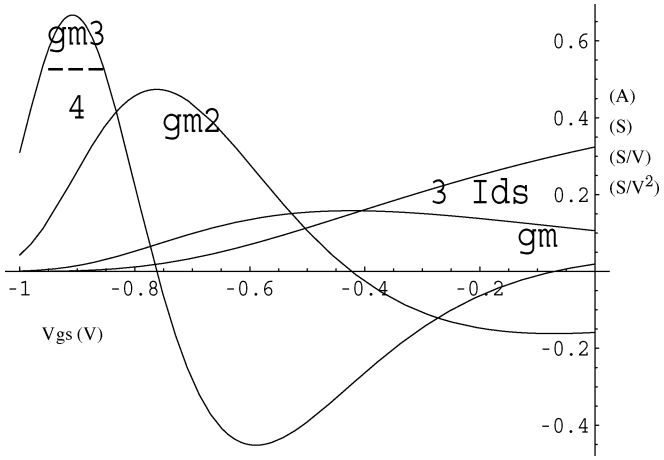

Fig. 4. Saturated drain current and its first three derivatives for the COBRA model indicating the model's excellent IMD predictive capability.

The COBRA expression, as indicated by Fig. 4, is globally continuous and is continuous to arbitrary levels of differentiation. This ensures a proper representation of a device's intermodulation characteristics for which higher order continuity is essential [10].

C. Nonlinear Charge Model

A computationally efficient and accurate nonlinear gate charge expression $Q(V_{\rm gs}, V_{\rm gd})$ has been formulated to model the bias dependencies of the junction capacitances for the GaAs pHEMT transistor [11]. The single charge function is dependent on the intrinsic terminal voltages $V_{\rm gs}$ and $V_{\rm gd}$ and obeys charge conservation since (3) is satisfied [12], [13] as follows:

$$\frac{\partial C_{\rm gs}}{\partial V_{\rm gd}} = \frac{\partial^2 Q}{\partial V_{\rm gd}\partial V_{\rm gs}} = \frac{\partial^2 Q}{\partial V_{\rm gs}\partial V_{\rm gd}} = \frac{\partial C_{\rm gd}}{\partial V_{\rm gs}}. \tag{3}$$

The adherence to charge conservation allows for the extraction of a consistent model with the complete absence of problematic transcapacitance elements [14]. Simplicity in the models structure lends itself to a more efficient and rapid parameter extraction.

The capacitances $C_{\rm gs}$ (4) and $C_{\rm gd}$ (5) are both derived from this same charge function and are interdependent with model parameters C_{pgs}, C_{pgd}, C_1, C_2, C_3, C_4, m, α_Q, λ_Q, and V_{to}.

$$\begin{aligned} C_{\rm gs}(V_{\rm gs}, V_{\rm ds}) &= C_{pgs} + \frac{C_1}{\left(1 - \dfrac{V_{\rm gs}}{V_{bi}}\right)^m} + C_2\left(1 + \tanh\left(\alpha_Q(V_{\rm gs} - V_{to})\right)\right) \\ &\quad + C_3(\operatorname{sech}\left(\alpha_Q(V_{\rm gs} - V_{to})\right) + \tanh(\lambda_Q(V_{\rm ds} - V_{to}))) \end{aligned} \tag{4}$$

$$\begin{aligned} C_{\rm gd}(V_{\rm gd}, V_{\rm ds}) &= C_{pgd} + \frac{C_1}{\left(1 - \dfrac{V_{\rm gd}}{V_{bi}}\right)^m} + C_2\left(1 + \tanh\left(\alpha_Q(V_{\rm gd} - V_{to})\right)\right) \\ &\quad - C_3\tanh\left(\lambda_Q(V_{\rm ds} - V_{to})\right) \\ &\quad - C_4\tanh(\lambda_Q V_{\rm gd})). \end{aligned} \tag{5}$$

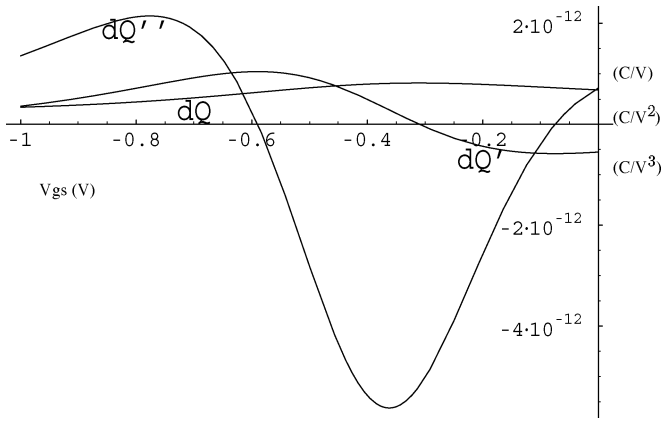

Fig. 5. Simulated derivatives of the single charge function for pHEMT model (with $V_{\rm ds} = 3$ V).

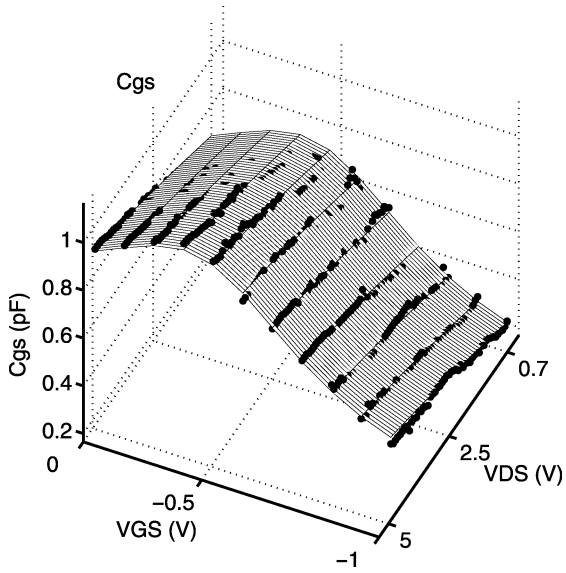

Fig. 6. Comparison of measured (dots) and modeled capacitance $C_{\rm gs}$ as a function of terminal bias voltages.

The single charge formulation and its respective derivatives are smooth and globally continuous, including into the pinchoff region, as is evident from the results of Fig. 5. This is of major importance as there is a strong relationship between large-signal model performance and higher order continuity of the charge model [15].

III. Large-Signal Model Validation

For the purpose of parameter extraction, dc and bias-dependent S-parameters measurements were performed on the packaged device. Deembedding and optimization took place using in-house software, which utilizes classical extraction theories [16]. The quality of the underlying extracted equivalent-circuit model topology is highlighted by the precision of the matches between the extracted and simulated voltage dependencies of the gate–source and gate–drain capacitances, as depicted in Figs. 6 and 7. The nonlinear pHEMT model was implemented in ADS using a symbolically defined device (SDD). This provides for its use and testing in RF circuit design. The model's intermodulation distortion (IMD) predictive

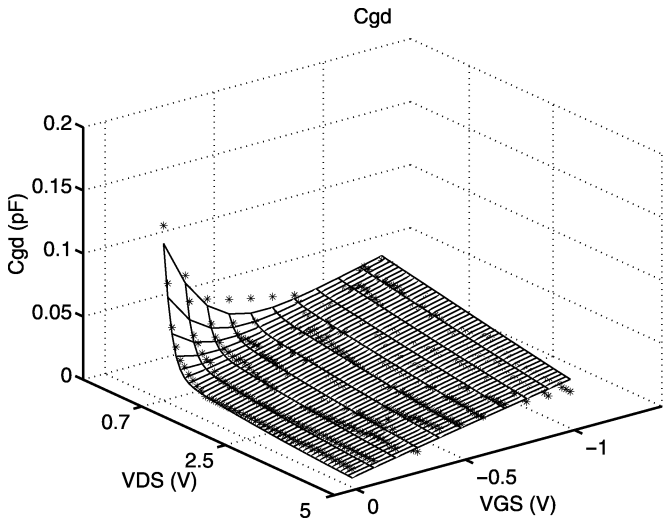

Fig. 7. Comparison of measured (dots) and modeled capacitance $C_{\rm gd}$ as a function of terminal bias voltages.

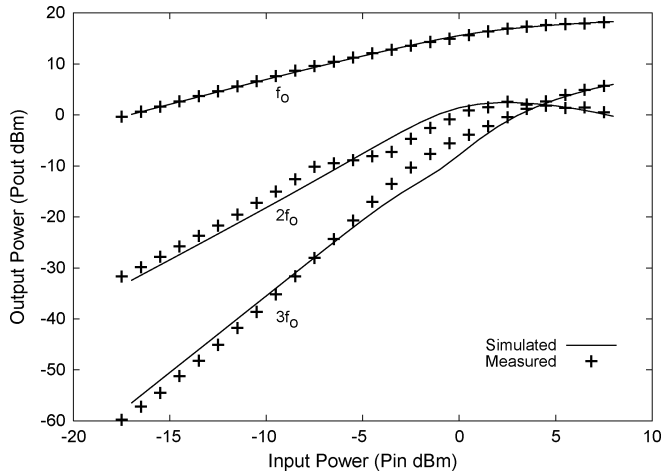

Fig. 8. Single-tone power measurements and ADS harmonic-balance simulation performance of proposed model at 2 GHz in a 50-Ω source and load impedance environment ($V_{\rm ds} = 3$ V, $V_{\rm gs} = -0.6$ up to third harmonic).

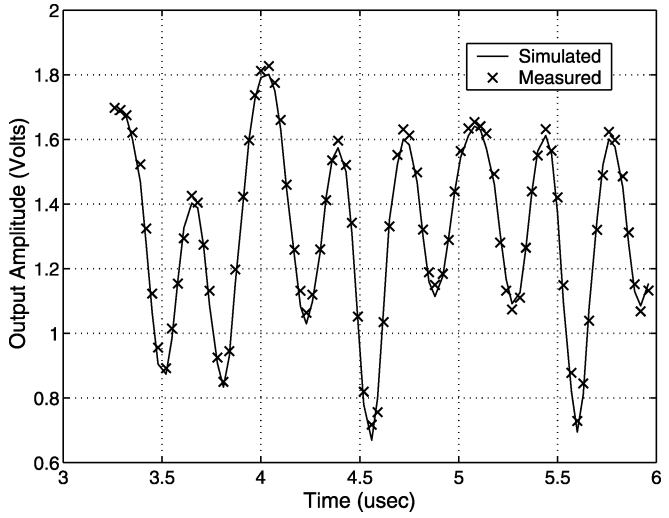

Fig. 9. Time-domain waveform amplitude of pHEMT output with W-CDMA input signal ($V_{\rm ds} = 3$ V, $V_{\rm gs} = -0.4$ V).

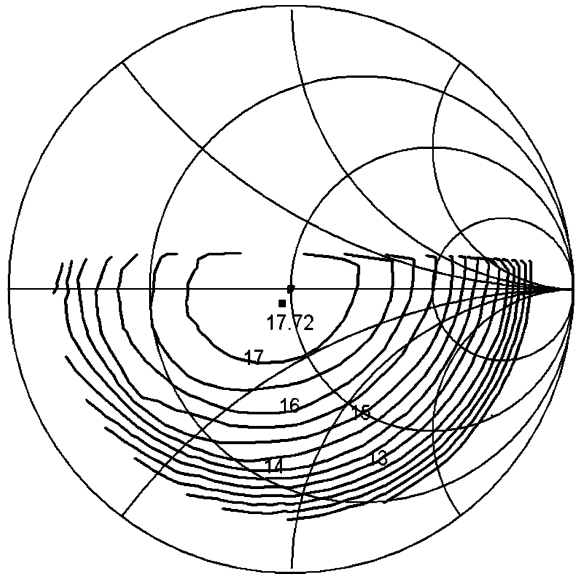

Fig. 10. Measured load–pull contours of output power (scale 0.5 dBm per contour) for pHEMT when driven at 3-dB compression point with 50-Ω source and biased at dc operating point of $V_{\rm ds} = 3$ V and $V_{\rm gs} = -0.2$ V.

capability has been presented separately [11], showing similar excellent agreement.

In order to validate the model, single-tone large-signal measurements were performed on the device at various dc-bias points covering the global dc-bias plane. The results of such a test are illustrated in Fig. 8, where excellent correlation between the simulated and measured results is displayed up to and including the third harmonic.

Having established the model's ability to predict with fidelity weakly nonlinear and strongly nonlinear distortion in the frequency domain using the harmonic-balance simulator, we sought to test our model with a real-world test signal. Utilizing ADS in a connected solution with an Agilent E4438C signal generator and an Agilent E4406A VSA, model performance testing in a real-world application environment has taken place. A 3GPP wireless code-division multiple-access (W-CDMA) signal at 2 GHz with a 3.84-M cps chip rate was generated and delivered to the input of the device with a 0-dBm power level. A sample of the output baseband time-domain waveform of the device is shown in Fig. 9. From these results, we can see that the waveform predicted by the extracted model has close agreement with the measured waveform, especially in the nonlinear region. The simulations were performed in ADS 2003A using the circuit envelope simulator and digital signal co-simulation.

An independent method of large-signal model validation is to use an experimental load–pull setup. Load–pull measurements were performed on the device using the ICM test fixture in connection with Focus Microwave's automated load–pull system. The results of such a test are displayed in Fig. 10, where the output power contours at 2 GHz are highlighted for the case where load is optimized for maximum output power for an input power corresponding to 3-dB compression. The maximum output power was measured to be 17.72 dBm at $0.922 - j0.092$, as indicated by the cross in this figure. The simulated results obtained from ADS show excellent

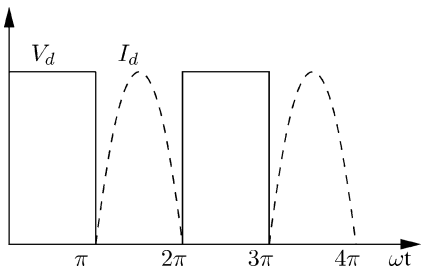

Fig. 11. Ideal drain voltage and current waveforms for the ideal class-F PA.

agreement, with a maximum output power of 17.84 dBm at $0.9316 - j0.0695$.

IV. Class-F PA Theory

A. Introduction

A class-F PA is based on a form of "waveform engineering," whereby an output filter is used to control the harmonic content of its drain–voltage or drain–current waveforms, thereby shaping them to reduce power dissipation by the transistor, thus increasing overall efficiency [17]. The transistor is also overdriven into compression in order to maximize efficiency and output power. The ideal class-F PA intrinsic drain output voltage and current waveforms are illustrated in Fig. 11. The ideal output is seen to consist of a square wave voltage waveform and the drain current is a half-wave rectified sinusoid [3].

Using simple Fourier analysis, it can be shown that a square waveform only has frequency components at its fundamental- and odd-order harmonics, while the half-wave rectified waveform only has fundamental- and even- order harmonic frequency components. A simple circuit topology, which, in principle, results in ideal behavior, consists of a resonator circuit, which presents an open termination at all odd harmonics and a short termination at all even harmonics [18]. The nature of the harmonic terminations constrain the harmonic powers $P_{out,nf}$ to be zero as $V_n I_n = 0$ for $n > 1$. Dissipation losses are also zero, as no waveform overlapping occurs, as highlighted by Fig. 11. The theoretical drain efficiency for this ideal configuration is, therefore, stated to be 100%.

However, in practice, an "approximation" to ideal performance takes place with circuits implemented with the required impedance conditions only for several harmonics. The complexity of a real PA is strongly dependent on the number of selective filters to be implemented. Furthermore, we have found that the filter design for controlling higher harmonics can become ineffective at high operating frequencies.

B. New Approach to Matching Network Design

A new theoretical methodology has recently been presented by Rhodes [4] in which the matching network elements for high-efficiency design are determined. This analysis is developed from the perspective of idealized circuit theory and is based on the premise that all that is needed to design a class-F RF PA is the proper choice of the parameters of the load network parallel circuit. It stipulates that the maximum efficiency of the circuit is obtained when its output equations are singular.

The transistor employed in this conjecture takes the form of a simple pHEMT model [2]. A singular solution to the class-F system equations [4, eqs. (1) and (33)] is proposed, where, depending on the number of harmonics being manipulated or controlled, there is a critical value for the complex impedance seen at the device output at the fundamental frequency that maximizes efficiency. The maximum efficiency is given by

$$\eta_d = \frac{2}{(m+1)} \cot\left[\frac{\pi}{2(m+1)}\right]. \tag{6}$$

The odd harmonics are open circuited up to the $(2m-1)$th harmonic with all even harmonics short circuited up to the $(2m-2)$th harmonic and harmonics greater than $2m$ considered to be related by a finite set of reactances $X(n)$.

The optimum complex impedance termination $Z_{\text{out,opt}}$ to be presented to the device output at the fundamental frequency is

$$\frac{2V_{\text{DC}}}{I_{\max}}(A_1 + jX_m) \tag{7}$$

where

$$A_1 = \frac{2}{(m+1)} \cot\left[\frac{\pi}{2(m+1)}\right] \tag{8}$$

$$X_m = \frac{I_{\max}}{\pi V_{\text{DC}}} \sum_{n=m}^{\infty} \frac{X(2n)}{(4n^2-1)} \frac{2n}{(m+1)} \cdot \left[\cot\left[\frac{(2n-1)\pi}{2(m+1)}\right] - \cot\left[\frac{(2n+1)\pi}{2(m+1)}\right]\right] \tag{9}$$

and $I_{\max}$ and V_{DC} are the maximum current and the dc drain voltage of the device, respectively.

The analysis in [4] continues with the synthesis of low-pass matching networks of characteristic impedance Z_0 developed to deliver this optimum impedance to the output of the transistor. The drain–source capacitance C_{ds} of the transistor is considered to be separable and is treated as part of the passive terminating network. The configurations of these networks are depicted in Fig. 12 for values of m up to the third degree. The element values in the circuits g_i alternate between shunt capacitance and series inductance. The explicit formulas for the elements of the general network are based on a cutoff frequency $\omega_c = 1$ and a reference impedance of 1 Ω and are derived using [4]

$$g_1 = 1 \quad g_r g_{r+1} = \frac{4}{(2m-1+r)(2m-r)}, \quad r = 2 \rightarrow 2m-1. \tag{10}$$

Table I summarizes the respective g values for the networks illustrated in Fig. 12.

This circuit architecture requires the user to optimize for the load impedance R_L and the shunt $L_T C_T$ tank resonator to ensure that correct impedance is transformed through the circuit to the device for optimum efficiency.

C. Idealized Model Simulations

In order to investigate the effectiveness of these novel load network topologies, simulations were performed in Agilent's ADS 2003A simulator. The assorted assumptions of the ideal transistor model were fully adhered to with the transistor being

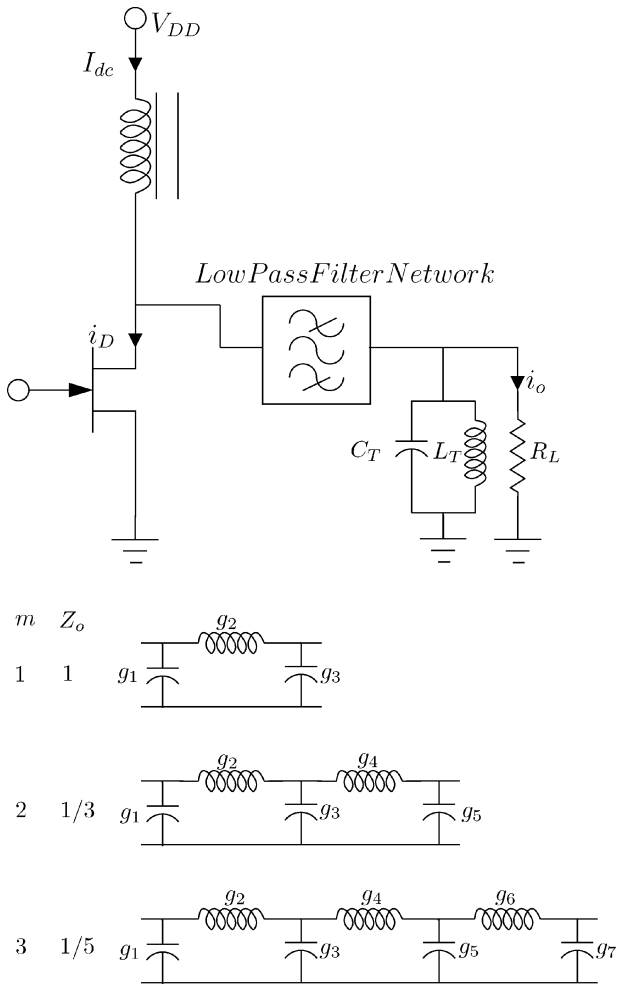

Fig. 12. Rhodes ideal low-pass matching networks for class-F PA design [4].

TABLE I
COEFFICIENTS FOR RHODES LOW-PASS MATCHING NETWORK

m	g_1	g_2	g_3	g_4	g_5	g_6	g_7
1	1	1	1				
2	1	$\frac{1}{6}$	$\frac{12}{5}$	$\frac{5}{18}$	$\frac{9}{5}$		
3	1	$\frac{1}{15}$	$\frac{15}{7}$	$\frac{7}{90}$	$\frac{20}{7}$	$\frac{7}{50}$	$\frac{50}{21}$

characterized by a simple Statz MESFET model operating at 850 MHz. The MESFET is given arbitrary dc operating values of $V_{\rm DC} = 5$ V and $I_{\max} = 2.5$ A and is biased near pinchoff with a gate–source bias of $V_{\rm GS} = -2.75$ V.

The circuit configuration for the seventh-order network is illustrated in Fig. 13. An RF choke is characterized by the quarter-wavelength ($\lambda/4$) transformer with a decoupling capacitor C_c in parallel. C_B is a dc blocking capacitor. This topology results in the second and fourth harmonics being short circuited and the third and fifth harmonics being open circuited at the drain of the transistor. When simulated in ADS using the harmonic-balance simulator, an optimum value of $\eta_d = 89.5\%$ is found for the maximum drain efficiency. The simulated drain current and drain voltage waveforms are displayed in Fig. 14.

The voltage waveform approximates a square wave, while the current is a half sine wave with deeply bifurcated current pulses. Circuit simulations of the matching network topology

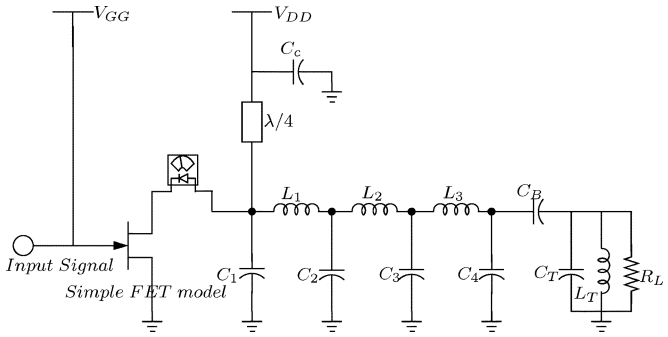

Fig. 13. Circuit topology for ideal class-F PA for $m = 3$.

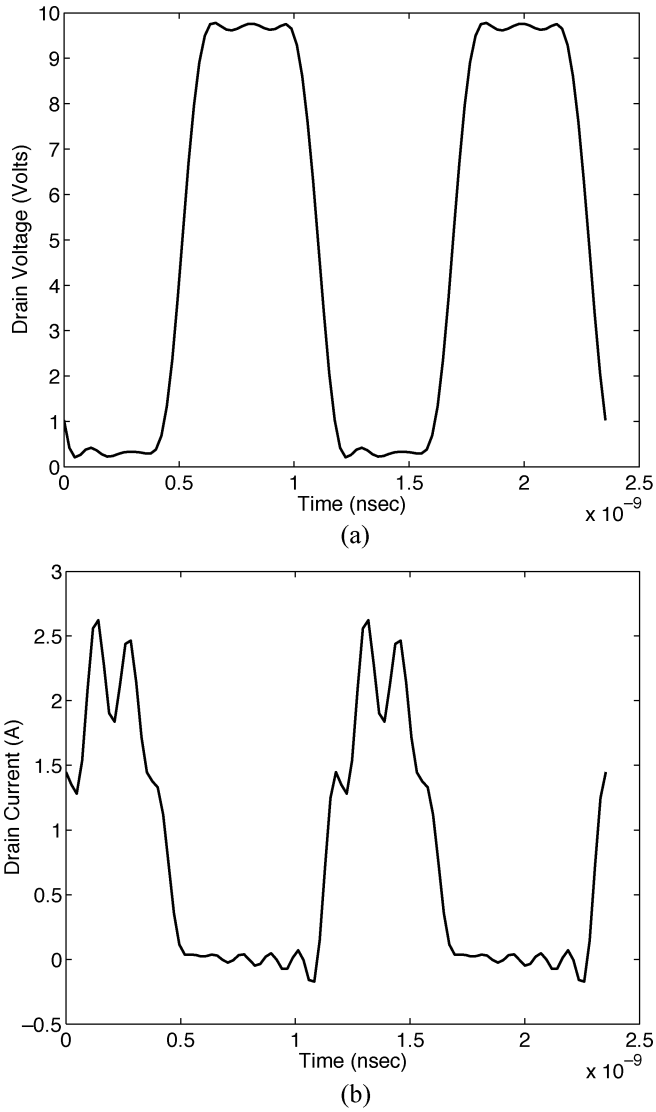

Fig. 14. Simulated class-F PA drain waveforms for ideal device case $m = 3$. (a) Voltage waveform. (b) Current waveform.

with values $m = 1, 2$ have also taken place. A comparison between the results recorded in these tests to those predicted from theory is denoted in Table II.

The efficiency figures presented here are very encouraging, but are based generally on some fundamental theoretical assumptions, which are not applicable for devices operating at high frequencies.

TABLE II
COMPARISON OF THEORETICAL AND SIMULATED MAXIMUM EFFICIENCY VALUES FOR IDEAL CLASS-F PA

m	$\eta_{Theory}(\%)$	$\eta_{ideal\ simulation}(\%)$
1	78.7	75
2	90.7	86.3
3	94.8	89.5

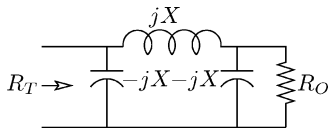

Fig. 15. Impedance inverter topology.

V. CIRCUIT DESIGN WITH NEW pHEMT MODEL

To utilize the theoretical methodology detailed above in a real-world design, some additional considerations had to be incorporated. The idealized picture is significantly altered for a real pHEMT device. Transistors, in general, have nonzero switching times and the output capacitance can be lossy at high-frequency levels. The presence of parasitic wiring inductances and package capacitances for a package device at these high frequencies has severe implications for harmonic terminations, especially as the ideal case requires that the open-circuit stubs be created at the ideal current generator or "virtual drain" ahead of the drain capacitance and package inductance and that the output capacitance be part of the load matching network [2].

The new large-signal model's excellence in predicting global nonlinear behavior of the Filtronic packaged pHEMT makes it very suitable for the class-F PA design. The hybrid PA was designed to operate at 2 GHz and, due to the complexity and sensitivity of the microstrip matching network at this frequency, a third-order PA design was used. A gate bias of -1 V with the drain at 5 V was selected to best meet the goal of optimum efficiency.

A. Initial Lumped-Component Design

Using the pHEMT SDD model in ADS, the value of the optimum complex impedance to be presented to the transistor to achieve optimum efficiency was determined to be $Z_{\text{out,opt}} = 113.8\,\Omega$. It was initially assumed that the impedance was real valued, i.e., $X_m = 0$, but tuning and optimization of the final circuit at later stages eventually makes $Z_{\text{out,opt}}$ complex valued. From inspection, the low-pass matching network topology in Fig. 12 is equivalent to the impedance inverter network of Fig. 15 whereby

$$R_T = \frac{X^2}{R_O}. \tag{11}$$

Using this information, the output circuit was synthesized to achieve impedance transformation from 50 Ω to the suitable fundamental and harmonic loads at the operating frequency of 2 GHz. Frequency and impedance scaling gave the initial lumped-component circuit of Fig. 16 with parameter values denoted in Table III.

The harmonic resonator described in theory is now realized using a quarter-wavelength transmission line, which operates as a harmonic short. The tuning of the network capacitance parameters sufficiently allows for the condition where the output package capacitance of the device is considered as part of the overall matching network. Using this ideal lumped-component circuit, a maximum simulated efficiency of $\eta_d = 72.88\%$ can be achieved in ADS harmonic-balance simulations.

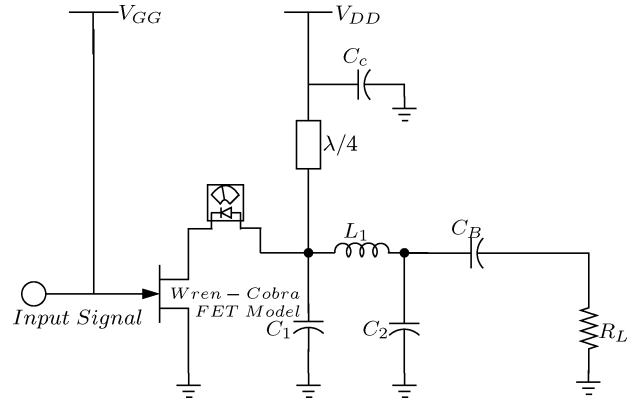

Fig. 16. Lumped class-F PA model.

TABLE III
LUMPED MATCHING NETWORK MODEL VALUES

C_1	L_1	C_2	C_c	R_L
1 pF	5.93 nH	1.06 pF	1.06 nF	50Ω

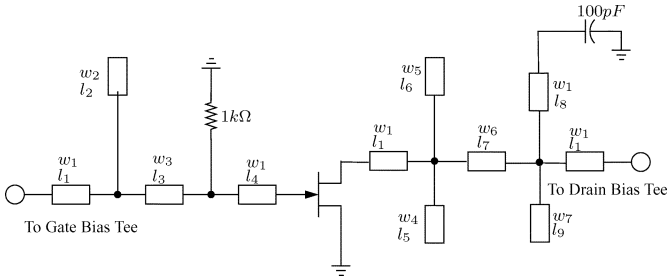

Fig. 17. Microstrip realization of PA input and output matching networks.

B. Microstrip Design

"Redundant" filter synthesis techniques that do not affect the output network response were used to convert the lumped representation to a more achievable and practical transmission line design [19]. The transmission-line impedances and electrical lengths of the matching network were optimized and tuned in ADS to simultaneously provide the correct impedance at the fundamental and also the required complex terminations. Simulations based on this virtual prototype circuit yield a maximum efficiency of $\eta_d = 74.5\%$ with the optimum fundamental complex impedance match now being $Z_{\text{out,opt}} = 112.89 - j12.14$.

An input matching network was determined, which, although not providing unconditional stability, does result in a stable environment for the loads and frequencies under consideration and a satisfactory level of small-signal gain. Both the input and load networks were converted to a tuned equivalent microstrip implementation and this final PA circuit can be seen in Fig. 17 with the respective microstrip widths and lengths contained in Tables IV and V.

TABLE IV
MICROSTRIP WIDTH VALUES (IN MILLIMETERS)

w_1	w_2	w_3	w_4	w_5	w_6	w_7
2.289	2.5	1.546	0.7248	0.839	0.659	1.826

TABLE V
MICROSTRIP LENGTH VALUES (IN MILLIMETERS)

l_1	l_2	l_3	l_4	l_5	l_6	l_7	l_8	l_9
6.07	18.42	19.2	5	4.72	5.09	14.15	27.84	13.77

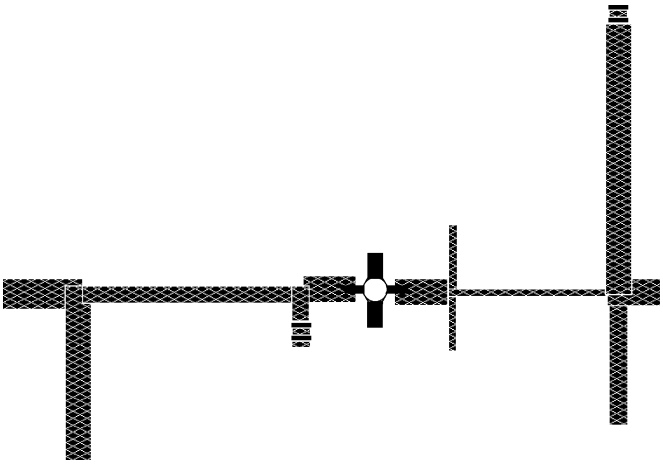

Fig. 18. Microstrip circuit layout of Fig. 17 including on-chip circuit components.

The microstrip substrate used was a low-loss Rogers 5880 Duroid ($\epsilon_r = 2.2, H = 0.75184$ mm). Extra 50-Ω lines were included in the matching network at the input and output terminals of the amplifier and transistor. These help reduce reflections that can result in power loss due to load mismatch. The positioning of the harmonic short in Fig. 17 was a difficult issue. Several different implementations were explored, but an optimal solution was found when placing it prior to the output launcher.

C. PA Layout and Results

In order to experimentally verify the proposed PA circuit topology, the single-ended PA was constructed using the ADS generated microstrip layout of Fig. 18. The pHEMT is the Filtronic LP6836P70 packaged pHEMT, as modeled in Section II.

Single-tone large-signal measurement tests, which utilize external dc-bias tees, were performed on the PA. The maximum efficiency obtained at the bias point of $V_{\rm ds} = 5$ V and $V_{\rm gs} = -1.0$ V when the amplifier was driven well into the saturation region was $\eta_d = 70.5\%$. The output power level measured at this point was $P_{\rm out} = 19.85$ dBm. This value compares very favorably with other published results and it is reasonably close to the optimum theoretical value of 78.7%. Tests taken at $V_{\rm ds} = 3$ V and $V_{\rm gs} = -1$ V recorded a maximum efficiency of 72% with a corresponding output power level of $P_{\rm out} = 16.02$ dBm.

The excellent performance of the active and passive model for the PA is clearly indicated in Fig. 19 where the drain efficiency and output power characteristics with varying input drive are compared for the measured and simulated cases. These results

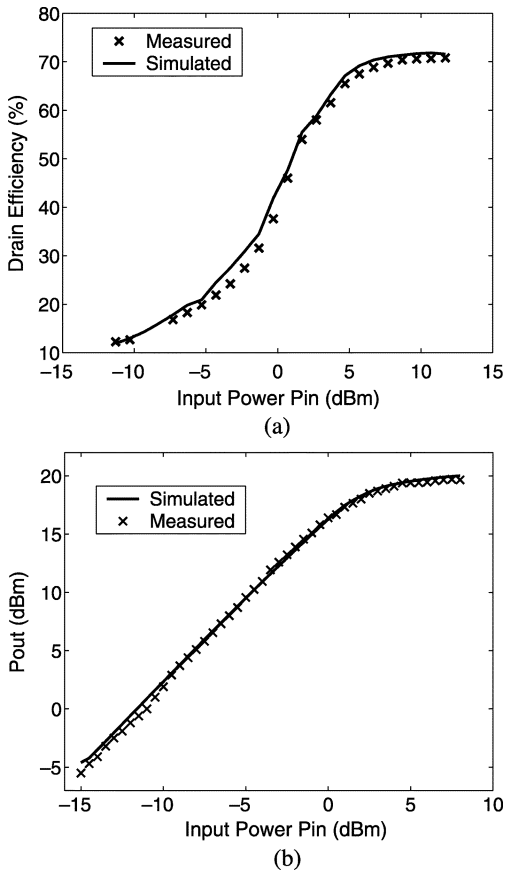

Fig. 19. Comparison between the measured and simulated: (a) drain efficiency η_d and (b) output power $P_{\rm out}$ of the class-F PA at 2 GHz with $V_{\rm ds} = 5$ V and $V_{\rm gs} = -1.0$ V.

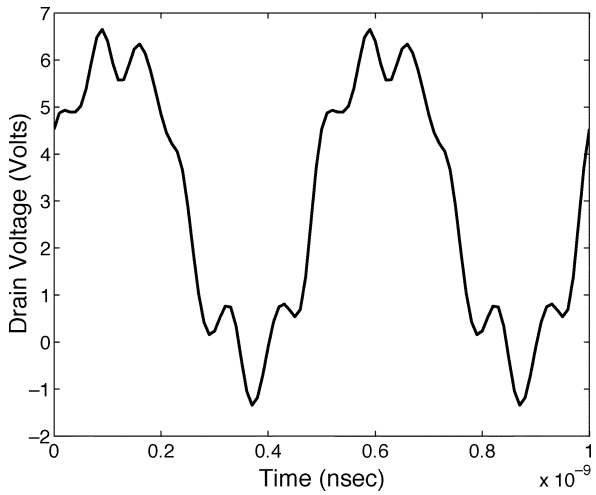

Fig. 20. Simulated intrinsic drain voltage waveform for PA when $\eta_d = 70.5\%$.

are even more remarkable considering the fact that no post-design tuning or adjustment has taken place.

The simulated drain voltage waveform of the class-F PA is shown in Fig. 20. The time waveform is seen to be very distorted and approximates the lumped class-F waveform behavior. A closer look at the spectral components of the output drain voltage of the PA in Table VI reveals behavior very similar to that of the ideal class-F case. The table exhibits a comparison

TABLE VI
COMPARISON BETWEEN MEASURED AND SIMULATED OUTPUT POWER $P_{\rm out}$ (IN dBm)

	P_f	P_{2nd}	P_{3rd}
Simulation	20.01	-31.56	-2.15
Measurement	19.85	-33.6	-3.21

between the measured and simulated output power $P_{\rm out}$ (up to and including the third harmonic) for the PA when driven with the input power level, which maximizes η_d at 2 GHz. The spectrum contains large amounts of odd harmonic frequency components, but even harmonic components are suppressed.

VI. CONCLUSION

In this paper, we have described the design of a high-efficiency class-F PA. The theories concerning the load network topology and design have been fully covered with a detailed analysis of the ideal theoretical performance presented. The novel network is shown to present the correct impedance required for optimum efficiency at the transistor output, as well as simultaneously suppressing the higher harmonics. A large-signal model for a GaAs pHEMT transistor has been introduced. The charge conservative and globally continuous model is shown to be well suited for RF circuit design. Model verification in both the time and frequency domains has taken place with excellent agreement obtained. Using this model, a class-F PA has been designed and fabricated in microstrip technology. A maximum efficiency of 70.5% was recorded at 2 GHz with the results highlighting that improved performance is achieved when utilizing an accurate model in the design process.

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