

# Large-signal modelling including low-frequency dispersion of n-channel SiGe MODFETs and MMIC applications

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## Abstract

This paper presents a circuit-design oriented, large-signal model for n-channel SiGe MODFET transistors, its application to the design of mixer and amplifier MMICs as well as measurement results. The model is based on an equivalent circuit approach and employs robust, globally continuous equations to describe the non-linear circuit elements. All transistor operating regions are covered without the use of partially defined equations or smoothing functions. Significant low-frequency dispersion effects similar to those found in III–V HEMT devices are observed and incorporated in a large-signal dispersion model. The bias dependency of the gate–drain and gate–source capacitance is extracted and modelled, allowing for verification of the model for frequencies up to 50 GHz. Based on the presented transistor model, an active FET mixer MMIC and a travelling-wave amplifier using the SiGe MODFET technology are designed and good agreement between simulation and measurements is achieved.

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## 1. Introduction

Modulation doped field-effect transistor (MODFET's) based on SiGe offer a new concept for an advanced high-frequency transistor, featuring similar performance advantages to the high electron mobility transistor (HEMT) in GaAs, but with the merits of low cost processing and compatibility with Si-based technologies. Devices with cutoff frequencies as high as  $f_T = 90$  GHz and  $f_{max} = 188$  GHz have been reported [1,2]. In order to make this promising technology

available for the design and realisation of high-speed circuits, an efficient non-linear simulation model is required which reliably predicts device behaviour. In this paper, we present the development of such a new large-signal equivalent circuit model together with its use in the design and realisation of the first monolithic microwave IC (MMICs) based on the SiGe MODFET technology.

Previous modelling work in conjunction with the new SiGe MODFET technology includes physical modelling and the extraction of small-signal equivalent circuit elements [3,4]. While physical modelling can provide valuable insight into the dependence of device RF properties on design parameters such as gate geometry and operating conditions (temperature etc.), this approach cannot provide the computational efficiency

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required for the simulation of integrated circuit networks. The aim of this work is to provide such an efficient, analytic large-signal model for use in circuit design. Therefore, the equations used for modelling the non-linear circuit elements are of a strictly empirical, non-physical nature, and model extraction relies heavily on numerical parameter optimisation, while physical interpretation and the possibility of direct parameter input, i.e. technology or measurable physical parameters, are deliberately sacrificed. However, the model does not contain any partially defined expressions, which makes it robust with respect to simulations requiring higher-order derivatives, e.g. intermodulation and harmonics generation evaluations.

Static and dynamic drain current characteristics can be well described using the COBRA FET model [7], developed at University College Dublin, which proves to be well suited for modelling purposes of SiGe MODFETs from the subthreshold to saturation regions. This is used as the basis of a complete non-linear equivalent circuit model, useful over the full gate- and drain-bias voltage plane.

After extracting the device's de-embedding parameters based on a standard circuit topology the non-linear gate capacitance and low-frequency dispersion model is developed. Small-signal values for the respective circuit elements are extracted at operating conditions over the whole bias plane. The voltage dependence of the gate-source and gate-drain capacitances thereby obtained, as well as the correction to transconductance and output conductance due to low-frequency dispersion effects, are here presented for the first time in conjunction with the SiGe MODFET technology. Large-signal representations of these effects are then developed and included in the model, which, implemented in a circuit design environment, allows for the design of integrated circuits using the SiGe MODFET technology.

## 2. The SiGe MODFET technology

The transistor used for characterisation and model parameter extraction is a  $0.1 \mu\text{m}$  gate length,  $100 \mu\text{m}$  gate width depletion mode n-channel MODFET [5,6]. The device has a  $\pi$ -shaped gate layout ( $\pi$ -gate) with two parallel gate fingers forming the total gate width. In the SiGe MODFET a two-dimensional electron gas (2DEG) forms in a strained-Si quantum well, sandwiched between two Sb-doped SiGe supply layers. All these layers have been grown by molecular-beam epitaxy. In order to form a relaxed SiGe layer acting as virtual substrate, a graded buffer is grown on the Si wafer. The complete layer sequence is shown in Fig. 1. The  $4 \mu\text{m}$  thick graded buffer grown by low energy plasma enhanced chemical

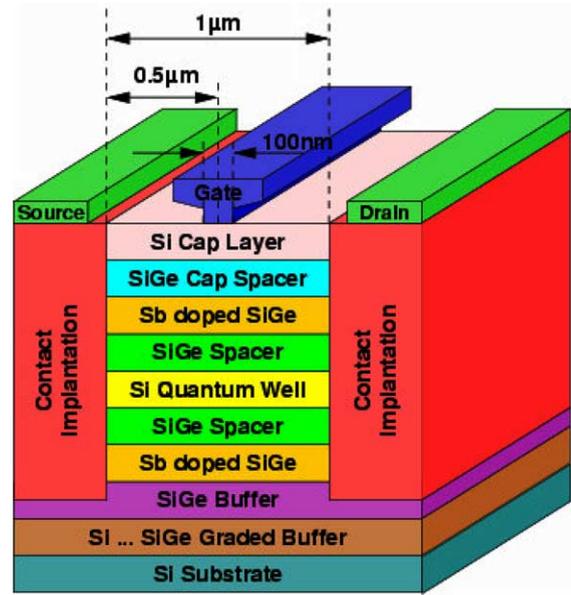


Fig. 1. Layer stack of the n-channel Si/SiGe MODFET.

vapour deposition (LEPECVD) has a final Ge content of 40%.

The embedded device's maximum transit frequency  $f_T$  and maximum frequency of oscillation  $f_{max}$  (defined via Mason's unilateral gain) are found to be 60 and 110 GHz, respectively. Typically, the device exhibits a threshold voltage of  $-0.7 \text{ V}$  and a maximum effective transconductance  $g_{m,max}$  of 240 mS/mm reached at a gate bias of  $-0.2 \text{ V}$ .

## 3. Large-signal model development

The equivalent circuit used for developing a large-signal model of the SiGe MODFET is shown in Fig. 2. It follows the typical FET topology, with the Schottky gate being modelled by two forward biased, non-ideal diodes ( $D_{gs}$  and  $D_{gd}$ ) distributed between the internal gate-drain and gate-source contacts. Gate current characteristics show non-negligible ohmic leakage, which is accounted for by using resistors placed in parallel to the diodes. Non-linear elements contained in the model are the static drain current source  $I_{ds}(V_{gs}, V_{ds})$ , a correction source  $I_{dss}(V_{gs}, V_{ds})$  accounting for the observed frequency dispersion effects and the voltage-dependent gate capacitance described by  $C_{gs}(V_{gs}, V_{ds})$  and  $C_{gd}(V_{gd}, V_{ds})$ .

### 3.1. Static/DC drain current

In a first step, the parasitic series resistance of the gate-, drain- and source contacts need to be extracted. The technique described in [9,10] has been employed to

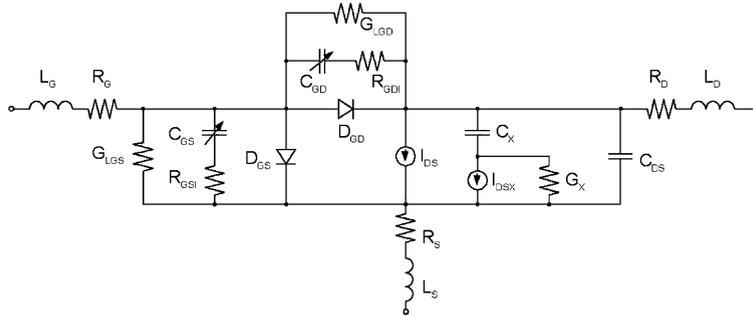


Fig. 2. Equivalent circuit model topology (excl. De-embedding network).

extract  $R_G$ ,  $R_D$  and  $R_S$  by means of device measurements under forward gate bias conditions. Considerable effort has been undertaken in the technological development of the SiGe MODFET structure to reduce the resistance of the drain and source implantation regions, e.g. by reducing the gate–source and gate–drain distance as well as by improving the quality of the metal-implantation interface. Nevertheless, the parasitic resistance of the drain and source contacts is still found to be  $9 \Omega$  for a  $2 \times 50 \mu\text{m}$  device, introducing severe voltage drop contributions due to the drain current and thereby reducing the maximum transconductance of the device from intrinsically  $320 \text{ mS/mm}$  to an effective  $g_m$  of  $240 \text{ mS/mm}$ .

The analytical COBRA model equations (1a)–(1d) [7] have been employed for the non-linear drain current source  $I_{ds}(V_{gs}, V_{ds})$ . In these expressions,  $V_{to}$  is the pinch-off voltage at low drain–source bias and  $\alpha, \beta, \gamma, \delta, \zeta, \lambda, \mu, \xi$  are fitting parameters which essentially have to be extracted using numerical parameter optimisation. In-house software based on the Levenberg–Marquardt optimisation algorithm is used for that purpose, its efficiency and stable convergence behaviour making it best suited for circuit element extraction.

$$I_{ds}(V_{gs}, V_{ds}) = \beta \cdot V_{\text{eff}}^{\lambda/\text{num}} \cdot \tanh(\alpha V_{ds}(1 + \zeta V_{\text{eff}})) \quad (1a)$$

$$\text{num} = 1 + \mu V_{ds}^2 + \xi V_{\text{eff}} \quad (1b)$$

$$V_{\text{eff}} = \frac{1}{2} \left( V_{gs} - V_{t1} + \sqrt{(V_{gs} - V_{t1})^2 + \delta^2} \right) \quad (1c)$$

$$V_{t1} = (1 + \beta^2)V_{to} - \gamma V_{ds} \quad (1d)$$

The COBRA expression is computationally very efficient. Mainly however, its single  $I_{ds}$  expression features continuous derivatives to infinite orders whereas partially defined expressions in many other empirical- or semi-empirical models rely on smoothing functions to assure continuous second-order derivatives. This makes the model very attractive for accurate prediction of

higher-order intermodulation behaviour as required in the evaluation of device linearity and frequency-translating effects.

Proving the model’s suitability in describing the SiGe MODFET, the transistor static drain current characteristics are measured over the complete  $I$ – $V$  plane and compared to the model, with gate–source voltages ranging from subthreshold to positive bias, and drain–source voltages covering the transistor’s linear and saturation operating regime. Fig. 3 shows the comparison of measured and modelled output characteristics.

### 3.2. Capacitance model

De-embedding of the internal transistor device, i.e. the subtraction of the coplanar contact pad parasitics is performed by means of OPEN and SHORT structures using standard de-embedding procedures. Using the technique described in [9] one can further reduce the de-embedded  $S$ -parameters of the internal transistor by the impact of the series resistance  $R_G$ ,  $R_D$  and  $R_S$ . This leads

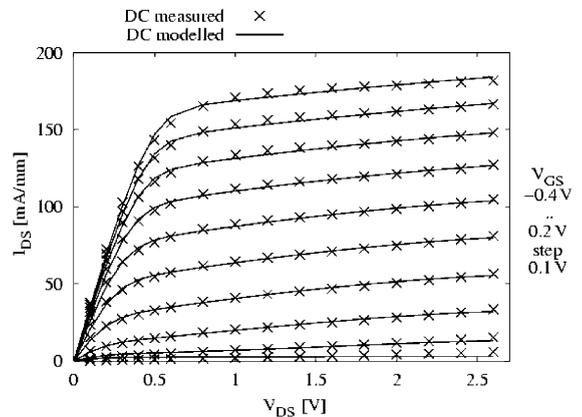


Fig. 3. Comparison of measured and modelled static output characteristics of a  $0.1 \mu\text{m}$  gate length,  $100 \mu\text{m}$  gate+width SiGe MODFET using the COBRA model expression.

to the intrinsic  $Y$ -parameter matrix of the device which can be solved to obtain the equivalent circuit parameters for every bias point using the equations developed in [11]. The smoothness of the obtained voltage-dependent data thereby serves as an indicator of the quality of the underlying equivalent circuit model topology.

The bias dependency of the gate–drain and gate–source capacitance obtained from multi-bias  $S$ -parameter data is the basis of the non-linear dynamic model. Despite the general modelling technique of using the derivatives of a channel charge expression to obtain branch capacitances, in this work an approach of directly modelling the extractable data, i.e. the branch capacitances, has been taken. This of course introduces the charge conservation issue [12] where the employed capacitance expressions, when derived from a single channel charge  $Q$ , need to fulfill condition (2) in order to assure charge conservation which otherwise can lead to simulation errors and convergence problems.

$$\frac{\partial C_{gs}}{\partial V_{gd}} = \frac{\partial^2 Q}{\partial V_{gd} \partial V_{gs}} = \frac{\partial^2 Q}{\partial V_{gs} \partial V_{gd}} = \frac{\partial C_{gd}}{\partial V_{gs}} \quad (2)$$

The empirical capacitance expressions presented in [13] have been used as a basis to model the voltage-dependence of the SiGe MODFET gate capacitance. A modification has been introduced to account for the particularities of the SiGe MODFET capacitance, but preserving charge-conservation. Eqs. (3) and (4) show the capacitance model employed.

$$\begin{aligned} C_{gs}(V_{gs}, V_{ds}) = & C_{pg} + \frac{C_{g1}}{\left(1 - \frac{V_{gs}}{V_{bi}}\right)^m} \\ & + C_{g2}(1 + \tanh(\kappa(V_{gs} - V_{to2}))) \\ & - C_{g3}(1 + \tanh(\iota(V_{gs} - V_{to3}))) \\ & + (C_{g4}(V_{gs} - V_{to4}) + C_{g5}) \tanh(\psi V_{ds}) \\ & + \frac{C_{g4}}{\psi} \log(\cosh(\psi V_{ds})) \end{aligned} \quad (3)$$

$$\begin{aligned} C_{gd}(V_{gd}, V_{ds}) = & C_{pd} + \frac{C_{g1}}{\left(1 - \frac{V_{gd}}{V_{bi}}\right)^m} \\ & + C_{g2}(1 + \tanh(\theta(V_{gd} - V_{to2}))) \\ & - (C_{g4}(V_{gd} + V_{ds} - V_{to4}) + C_{g5}) \tanh(\psi V_{ds}) \end{aligned} \quad (4)$$

The first term in these expressions (parameters  $C_{pg}$ ,  $C_{pd}$ ) allows for a bias-independent overlap capacitance between gate–source and gate–drain. The second term (parameters  $C_{g1}$ ,  $V_{bi}$ ,  $m$ ) is the well-known diode capacitance expression, followed by empirical expressions to account for additional bias dependency of the terminal capacitances. Here, parameters  $V_{to2}$ ,  $V_{to3}$ ,  $V_{to4}$  represent the approximate transition between voltage operating

regimes, namely subthreshold to conduction, 2DEG to 3DEG channel formation (see below) and linear to saturation regime, respectively. Greek characters  $\iota$ ,  $\kappa$ ,  $\psi$  describe the shape of the transition, while  $C_{g2}$  through  $C_{g5}$  model the magnitude of capacitance change between the operating regimes.

The resulting match of extracted and modelled voltage dependence of the gate–source and gate–drain capacitance is shown in Figs. 4 and 5, respectively.

A peculiar dependence of the gate–source capacitance against  $V_{gs}$  is found (Fig. 6). Contrarily to the typical HEMT behaviour of increasing  $C_{gs}$  and decreasing  $g_m$  with increasing  $V_{gs}$  due to the formation of the parasitic MESFET channel in the front-side supply layer, here  $C_{gs}$  decreases together with  $g_m$ . An explanation for this behaviour might be the formation of a first parasitic MESFET channel (with less carrier mobility) in the supply layer underneath the strained-Si quantum well, increasing the effective gate-channel distance and thereby reducing  $C_{gs}$ .

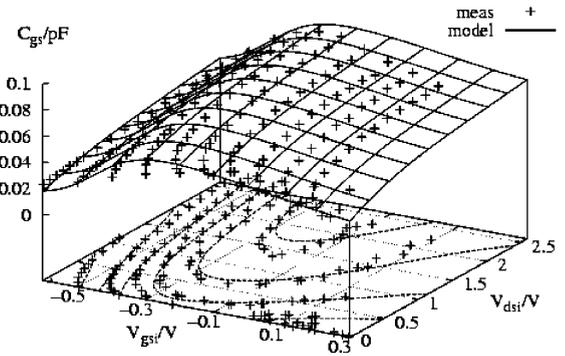


Fig. 4. Comparison of extracted and modelled gate–source capacitance as a function of intrinsic terminal bias voltages.

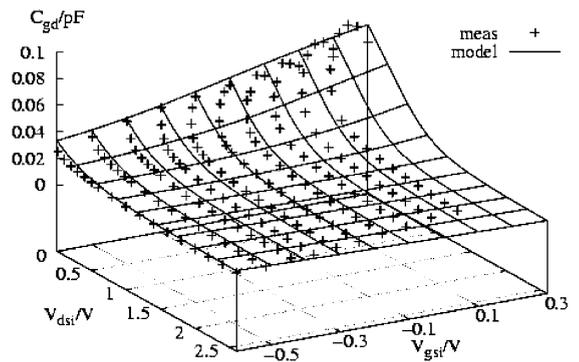


Fig. 5. Comparison of extracted and modelled gate–drain capacitance as a function of intrinsic terminal bias voltages.

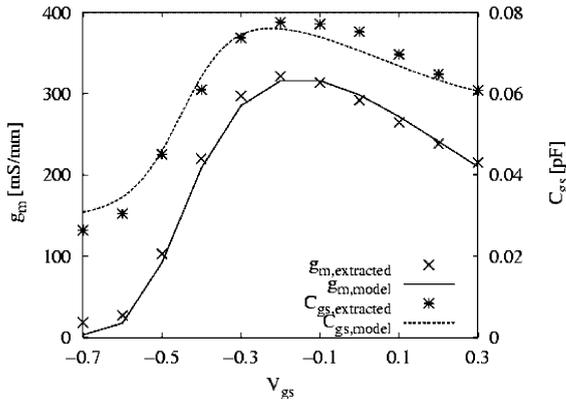


Fig. 6. Transconductance and gate–source capacitance as a function of gate bias,  $V_{ds} = 1.2$  V.

### 3.3. Low-frequency dispersion model

Low frequency dispersion, i.e. the difference between static and dynamic device characteristics, is a well investigated phenomenon in HEMT devices based on GaAs, InP and GaN. Physically, frequency dispersion effects arise from the presence of charge traps in the channel region, capturing and releasing carriers with an associated time constant, thereby modifying the available channel carrier density. Additionally, self-heating effects, where the power dissipation at high drain- and gate-potentials in the device leads to temperature related altering of carrier mobility, introduce frequency dependence of drain current. Finally, surface states at layer interfaces may show frequency dependent occupation behaviour and contribute to a modification of the effective gate potential. Typically, these so-called low-frequency dispersion effects are characterised by means of pulsed  $I$ - $V$  measurements, but can also be deduced from  $S$ -parameter measurements carried out well above the critical frequencies, thereby revealing a discrepancy between static and dynamic trans- and output conductance.

Although dispersion results mainly in a reduction of transconductance and an increase in output conductance with increasing frequency, the effect on the input characteristics due to surface charges has also been observed and modelled [8]. From a modelling point of view, the bias-dependent altering of  $g_m$  and  $g_{ds}$  at high frequencies needs to be included.  $S$ -parameter measurements of the SiGe MODFET clearly indicate the presence of dispersion in these Si-based devices, with transconductance being decreased by up to 10% and output conductance being increased by up to 200% at frequencies exceeding the MHz regime (Figs. 7 and 8). Both parameters have been extracted for frequencies exceeding 1 GHz, where the influence of dispersive effects on small-signal characteristics is avoided. While transconductance is affected

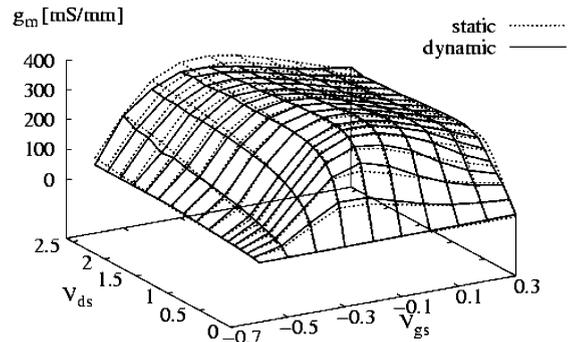


Fig. 7. Static and dynamic intrinsic transconductance as a function of applied bias voltage.

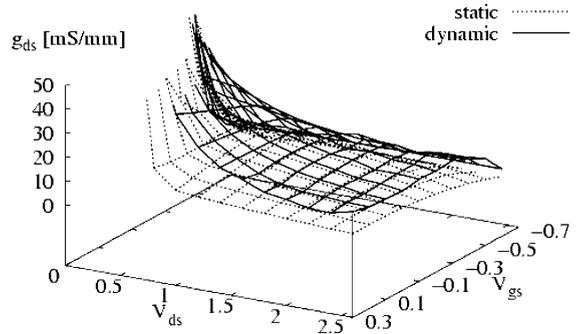


Fig. 8. Static and dynamic output conductance as a function of applied bias voltage.

only for large  $V_{ds}$  values, the device output conductance shows frequency dispersion over the whole  $I$ - $V$  plane. Output conduction dispersion is mainly due to the thermal or self-heating effect, in addition to deep-level traps and surface states. The self-heating related altering of output conductance observed in DC characteristics does not occur in  $S$ -parameter measurements. Thermal conductivity of the substrate and the relaxed buffer play a major role here. While the effect of self-heating on DC characteristics is considerable in the SiGe MODFET, it is still less pronounced than in GaAs HEMT devices, indicating a substantially higher thermal conductivity of the  $\text{Si}_{0.6}\text{Ge}_{0.4}/\text{Si}$  combination. Although undoped  $\text{Si}_{0.6}\text{Ge}_{0.4}$  has a very low thermal conductivity of  $\kappa = 0.08$  W/(cm K) [14], the relatively thin relaxed SiGe buffer and spacer layers do not impose a severe limitation on the device's thermal behaviour.

Applying the same technique used to obtain capacitance data, one obtains the dynamic trans- and output conductance of the device from solving the intrinsic  $Y$ -parameters  $Y_i$  for the respective circuit elements. For moderate frequencies up to a few GHz, one can apply

$$g_{\text{mac}} = \text{Re}(Y_{21i}), \quad g_{\text{dsac}} = \text{Re}(Y_{22i}) \quad (5a, b)$$

while the static trans- and output conductance is of course obtained via

$$g_{\text{mdc}} = \frac{\partial I_{\text{dsdc}}}{\partial V_{\text{gs}}}, \quad g_{\text{dsdc}} = \frac{\partial I_{\text{dsdc}}}{\partial V_{\text{ds}}} \quad (6a, b)$$

Integration of dynamic trans- and output conductance then allows for the introduction of the dynamic large-signal  $I$ - $V$  characteristics  $I_{\text{dsac}}(V_{\text{gs}}, V_{\text{ds}})$ , shown in Fig. 9. As the independently extracted  $g_{\text{mac}}$  and  $g_{\text{dsac}}$  do not necessarily constitute the gradient field of a drain current  $I_{\text{dsac}}$ , an additional optimisation step is required to obtain an  $I_{\text{dsac}}$  whose linearisation will best fit the extracted small-signal parameters. The current source  $I_{\text{dsx}}(V_{\text{gs}}, V_{\text{ds}})$  contained in the model is implemented as

$$I_{\text{dsx}}(V_{\text{gs}}, V_{\text{ds}}) = I_{\text{dsac}}(V_{\text{gs}}, V_{\text{ds}}) - I_{\text{dsdc}}(V_{\text{gs}}, V_{\text{ds}}) \quad (7)$$

It should be stressed that the dynamic  $I$ - $V$  characteristics are not measured directly, as would be the case in pulsed  $I$ - $V$  measurements, but reflect the measured dynamic trans- and output conductance.

In conjunction with the DC blocking capacitor  $C_X$  and the minimum conductance  $G_X$  necessary for DC convergence, it creates the correct dynamic  $I$ - $V$  characteristics above a certain corner frequency. The corner frequency for the transition between static and dynamic  $I$ - $V$  characteristics is set by appropriately choosing the values of  $C_X$  and  $G_X$ .

With the inclusion of dispersion- as well as capacitance models, validation can be carried out for both DC and high-frequency. Fig. 10 shows the comparison of measured and simulated  $S$ -parameters for frequencies up to 50 GHz using the full non-linear model.

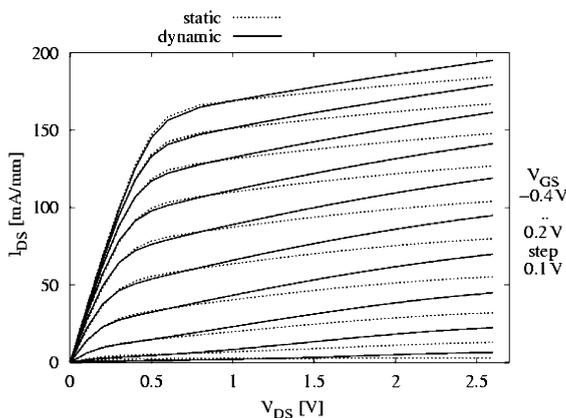


Fig. 9. Dynamic  $I$ - $V$  characteristics obtained from integration of trans- and output conductance compared to the static curves.

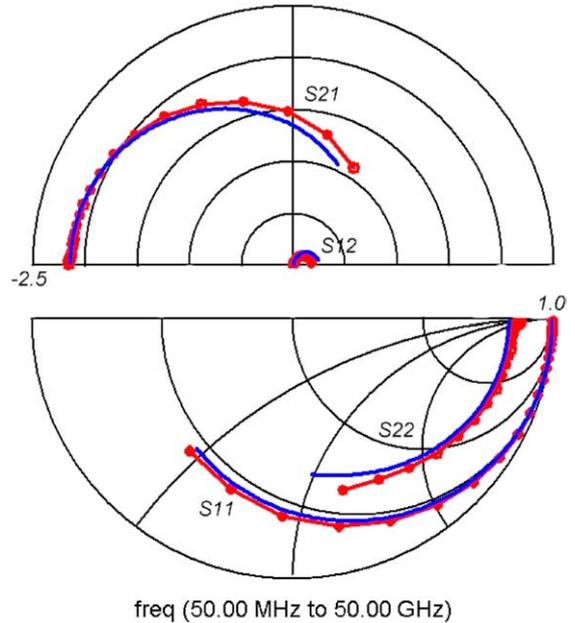


Fig. 10. Measured (dotted) and modelled (straight)  $S$ -parameters of the SiGe MODFET. Bias conditions are  $V_{\text{gs}} = -0.2$  V,  $V_{\text{ds}} = 1.6$  V.

#### 4. MMIC design and realisation

The large-signal model for the SiGe MODFET presented in the preceding chapters has been implemented in the ADS simulation environment and can be employed in time- and frequency domain simulation techniques. It serves as the basis for the design of the first SiGe MODFET monolithic integrated circuits, namely an active FET mixer and a travelling-wave amplifier.

##### 4.1. Active FET mixer

Prediction of the frequency-translating effect exploited in mixer applications requires accurate and computationally efficient large-signal model describing the non-linearities in the devices involved. A single-balanced active FET mixer MMIC using the SiGe MODFET technology has been designed and simulated based on the presented large-signal model [15]. The SiGe MODFET is an interesting candidate for the design of mixing applications due to its high-frequency and RF power capabilities.

Fig. 11 shows the schematic of the mixer. It uses a half Gilbert cell topology, with the differential LO signal being applied to the upper transistors of a differential stage, which act as current switches. The lower transistor acts as a common-source amplifier to the RF signal. Fig. 12 shows the layout of the realised mixer. In very good agreement with the simulated results, a conversion loss

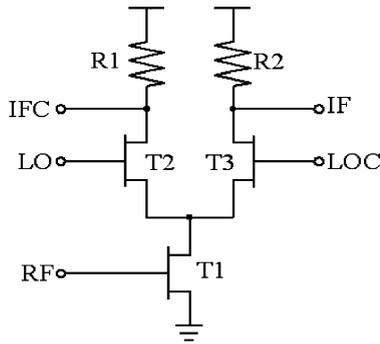


Fig. 11. Schematic of the active FET mixer.

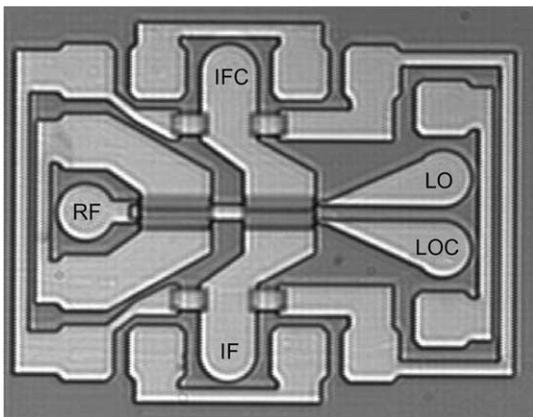


Fig. 12. Microphotograph of the active FET mixer MMIC design.

of 4.0 and 4.6 dB has been achieved for down-conversion of 3.0 and 6.0 GHz RF signals, respectively, to an intermediate frequency of 500 MHz using high-side injection of 5 dBm LO power (Fig. 13).

#### 4.2. Travelling-wave amplifier

To further exploit the SiGe MODFET's high-frequency operation capabilities, the design of a broad-

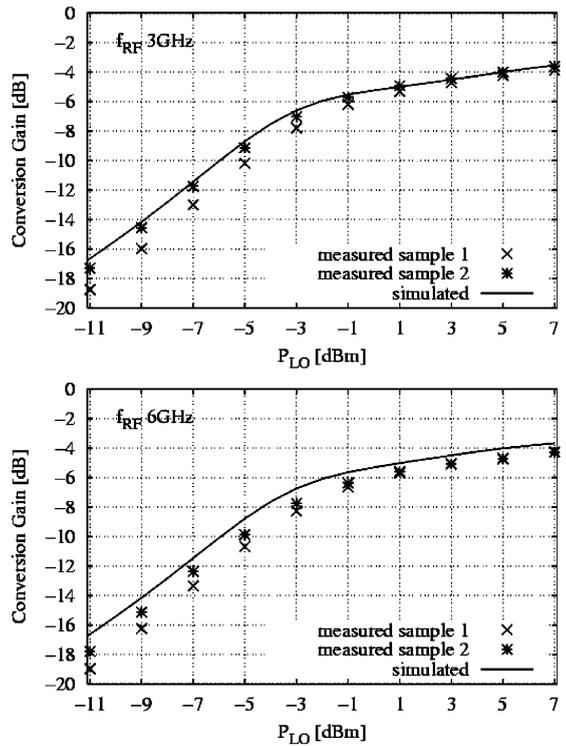


Fig. 13. Comparison of measured and simulated conversion gain versus LO power for down-conversion a 3 GHz (a) and 6 GHz (b) signals to an IF of 500 MHz.

band amplifier MMIC in the form of a travelling-wave or distributed amplifier has been undertaken [16]. In the travelling-wave amplifier principle, the amplifying transistor cells are embedded into artificial 50 Ω transmission lines, thereby allowing for ultra-broadband operation and excellent input and output matching characteristics. Such a design crucially depends on accurate modelling of the transmission lines as well as the reactive transistor characteristics, mainly the gate–source, gate–drain and drain–source capacitance. For the active parts of the amplifier, the above presented large-signal transistor model was employed, whereas a special coplanar

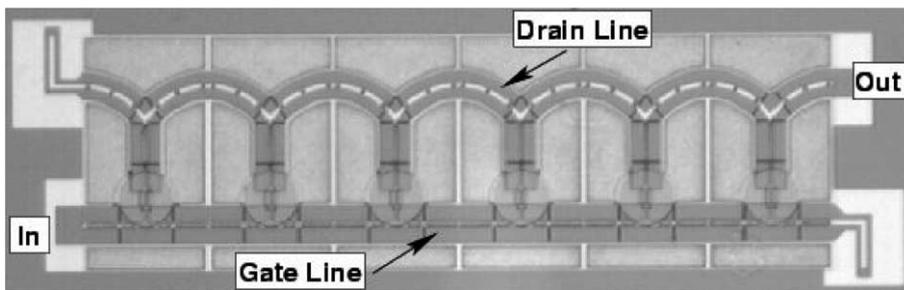


Fig. 14. Layout of a travelling-wave amplifier using six common-source amplifying stages.

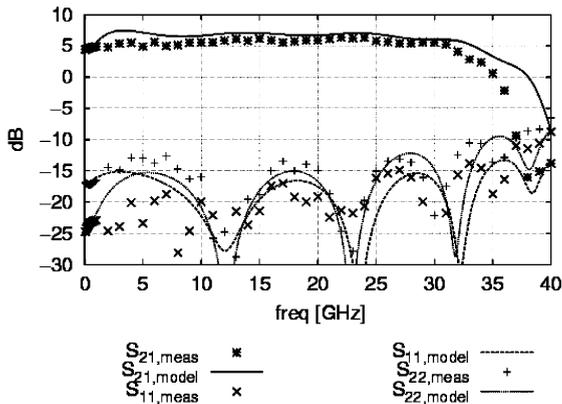


Fig. 15. Comparison of measured and modelled  $S$ -parameters (gain and in-/output reflection) of the six-stage TWA.

waveguide model was developed for the SiGe technology using test structures on epitaxially similar test wafers. Here, the use of a non-linear transistor model allows for the optimisation of bias conditions in the amplifying stages.

Fig. 14 shows the layout of a six-stage travelling-wave amplifier using common-source amplifying stages. In good agreement with simulation it achieved a flat gain of 5.5 dB over a 32 GHz bandwidth for bias conditions of  $V_{gs} = -0.17$  V,  $V_{ds} = 2.3$  V (Fig. 15). It should be noted that this design, in contrast to the mixer MMIC, requires a second metallisation layer to provide MIM capacitance and cross-overs in the CPW lines.

## 5. Conclusion

A large-signal model for the SiGe MODFET technology has been introduced, containing a drain current model valid over the whole  $I$ - $V$  plane as well as a novel non-linear, charge-conservative capacitance model. Frequency-dispersive effects are observed and included in the model to obtain dynamic  $I$ - $V$  characteristics.  $S$ -parameter verification is carried out for frequencies up to 50 GHz. The model offers computationally efficient, globally continuous equations and is well suited for the design of microwave circuits.

Based on this simulation model, the SiGe MODFET technology could successfully be demonstrated in the design, simulation and fabrication of an active FET mixer MMIC and a travelling-wave amplifier application. Considering the technological improvements expected to further boost the SiGe MODFET's capabilities in terms of speed, linearity and power at microwave frequencies, these results are strongly encouraging the design of more sophisticated circuits in the field of analog high-speed front-ends.

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